DEPARTMENT OF THE ARMY TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL, DS, GS AND DEPOT MAINTENANCE MANUAL

RADIATION INCORPORATED DAS-10 DISTORTION ANALYZER SYSTEM

This copy is a reprint which includes current pages from Changes 1 and 2.

HEADQUARTERS, DEPARTMENT OF THE ARMY
SEPTEMBER 1969

WARNING

Be careful when working on the 115-volt ac line connections. Serious injury or death may result from contact with these terminals.

CAUTION

Insertion of excessive dc voltages into the rear input connections (J2) of Data Transmitter 7413A, and to the HIGH Z INPUT jack of Data Analyzer 7422 will cause excessive damage to modules. Observe connections at dc patch boards.

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PART A
SECTION I

INTRODUCTION

1-1. Scope

This manual described the DAS-10 Distortion Analyzer System Model 7010 which consists of Models 7413 and 7413A Data Transmitter, Model 7422 Data Analyzer, and Model 7431 A-Scan manufactured by Radiation Incorporated. It includes operating instructions, installation, and troubleshooting procedures. Each equipment is described in a separate part of the manual.

NOTE

Appendix B is current as of 13 September 1969.

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to DA Pam 310-7 for modification work orders pertaining to the equipment.

1-3. Forms and Records

a. Reports of Maintenance and Unsatisfactory Equipment. Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38-750.

b. Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 (Report of Packaging and Handling Deficiencies) as prescribed in AR 700-58 (Army)/NAVSUP PUB 378 (Navy/AFR 71-4 (Air Force)/and MCO P4030-29 (Marine Corps).

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38 (Army)/NAVSUP PUB 459 (Navy)/AFM 75-34 (Air Force)/and MCO P4610.19 (Marine Corps).

1-3.1. Reporting of Errors

Report of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028, Recommended Changes to Publications, and forwarded direct to Commander, US Army Electronics Command, ATTN: AMSEL-MA-C, Fort Monmouth, NJ 07703.

1-4. Purpose

The Data Transmitter, Model 7413 (figure 1-1), is a compact, portable, solid-state device, designed to produce a known message, with controlled distortion, at rates up to 9600 bits per second to check the operation of telegraph and data transmission systems.

1-5. General

The Data Transmitter incorporates either of two card-selected formats: (1) a standard 880-haracter "Fox" message in five-unit Baudot code; (2) an 8-bits-percharacter, 90-character pattern with internal provision for less than 8-bit code. There is also a single, repetitive, switch-selected character of five, six, seven or eight information bits in any combination of marks and spaces, and an internally selected idle character.

The generated format may be transmitted as START-STOP; or as synchronous, five, six, seven or eight bits per-character.

External timing input is provided for character-bycharacter or bit-by-bit release of the selected format.

Also, clock provided by the Model 7422 Analyzer permits continuous transmission at a switchselected rate. Alternate mark and space elements may be generated at the selected rate, and continuous-mark and continuous-space conditions are selectable.

Figure 1-1. Data Transmitter, Model 7413

Distortion of the generated format is accomplished digitally. The type of distortion may be switched manually or automatically.

Non-standard formats of up to 128 characters, arranged as required, are available on request.
Non-standard speeds, from 10 to 9600 bits per second, are available on request.

1-5.1. Items Comprising an Operable Radiation Incorporated DAS-10 Distortion Analyzer System.

FSN	QTY	NOMENCLATURE, PART NO., AND MFR CODE	FIG. NO.
6625-930-8525		Radiation Incorporated; DAS-10; Distortion Analyzer System consisting of:	
		NOTE **The part number is followed by the applicable 5-digit Federal supply code for manufacturers (FSCM) identified in SB 70842 and used to identify manufacturer, distributor, or Government Agency, etc.**	
	1	Analyzer, 7422, 91417	1-1
	1	XMTR., 7413, 91417	1-1
	1	1A1, Scan, 7431, 91417	3-1

1-6. Technical Characteristics

1-7. Type of Output Signals

(*a*) *Polar of Neutral*. Solid-state keying circuitry (dry contact), capable of keying 100 milliamperes maximum. (Maximum contact resistance is approximately 75 ohms at 20 ma Voltage rating is 260 volts maximum for neutral operation, and +130 volts maximum for polar operation. Contacts are fused at 1/8A. (Fuses are accessible from near panel.)

(*b*) *Standard Interface Output*. A polar signal +6 volts (mark = +6 volts, space = -6 volts) into 600-ohm load, with external +6V and 6V supplies.

1-8. Bias Distortion (Rotary Switch)

(1) ZERO (perfect data)
(2) MARKING (distortion)
(3) SPACING (distortion)
(4) SWITCHED (distortion)

(5) PERCENT DISTORTION (indicating thumbwheels)

Distortion is controlled in 1% increments from zero to 49%. In switched distortion, the type of distortion is automatically switched with each character transmitted with alternating mark bias or space bias distortion.

1-9. BAUD RATE (Rotary Switch)

Twelve standard baud rates internally generated are: 45.50, 50.00, 55.60, 61.12, 75, 150, 300, 600, 1200, 2400, 4800 and 9600 bauds per second, accurate to +0.1%, with a stability of one part in 10,000 for 30 days.

1-10. CODE LEVEL (Rotary Switch)

START-STOP or SYNC transmission of the selected format at 5, 6, 7 or 8 bits per character are switch-selected.

1-11. PATTERN SELECTOR (Rotary Switch)

(1) REVERSALS -	Causes alternate marks and spaces to be generated at the selected bit rate.
(2) SELECTED CHARacters -	A character of 5, 6, 7 or 8 information bits which is selected by front-panel pushbuttons.
(3) IDLE CHARacter -	Same as selected character but programmed by internal slide switches.
(4) TEST MESSAGE -	Baudot code to ASCII code may be effected by card change. (ASCII —

American Standard Code for Information Interchange)

Baudot; - a message in five-unit code of up to 128 characters. Standard message "THE QUICK BROWN FOX JUMPS... . "etc. ASCII; - up to 128 characters of up to 8 information bits per character.

1-12. RELEASE INFORMATION (Rotary Switch)

(1) BIT SYNChronization	Allows the selected format to be transmitted at a bit rate determined by an external timing signal.
(2) FREE RUN -	Causes the selected format to be transmitted continuously at the selected bit rate.
(3) STEPPED -	Allows the selected format to be transmitted at a character rate determined by external timing signal, with bit rate determined by front-panel switching.
(4) STEADY MARK -	Causes a continuous mark to be generated.

1-13. STOP PULSE LENGTH CONTROL

The length of the STOP element is controlled in 0.01 unit increments from

1.00 units to 2.00 units by internal slide switches.

1-14. TEMPERATURE

The Data Transmitter operates from 0 degrees C to 50 degrees C.

1-15. CONSTRUCTION

The Transmitter construction conforms with best commercial standards fully transistorized - with plug in modules. The modules are standard "off-the shelf" items. Modules with the same part number can be interchanged with no adjustment. The very high reliability rating (high MTBF) of these modules reduces maintenance and down time to a minimum.

1-16. MOUNTING

The unit may be used as a portable test equipment, or can be rack-mounted in a standard 19-inch rack.

1-17. DIMENSIONS

The unit is 3-1/2 inches high, 17-1/2 inches wide, 18 inches deep.

1-18. WEIGHT

The unit weighs approximately 19 1/2 pounds.

1-19. POWER REQUIREMENTS

The Transmitter requires (+) and (-) 10 volts derived from the Analyzer.

1-20. ACCESSORIES

The following accessories are available for use with the Model 7413 Data

Transmitter:

(1) Module Remover, Model 106338-1 (Figure 1-2)

(2) Rack Mounting Kit, Model 74124 (Figure 1-3)

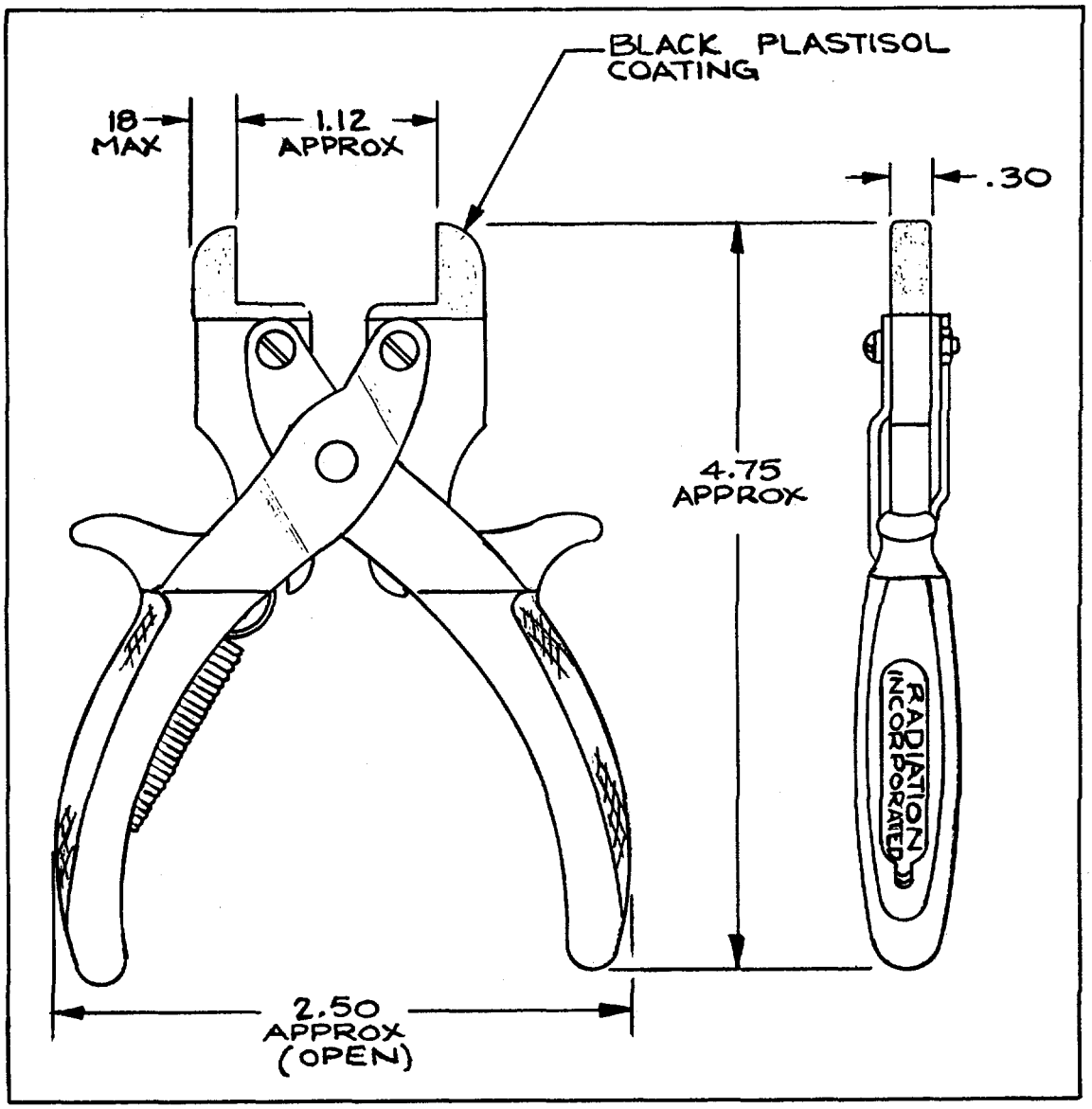


Figure 1-2. Module Remover, Model 106338-1

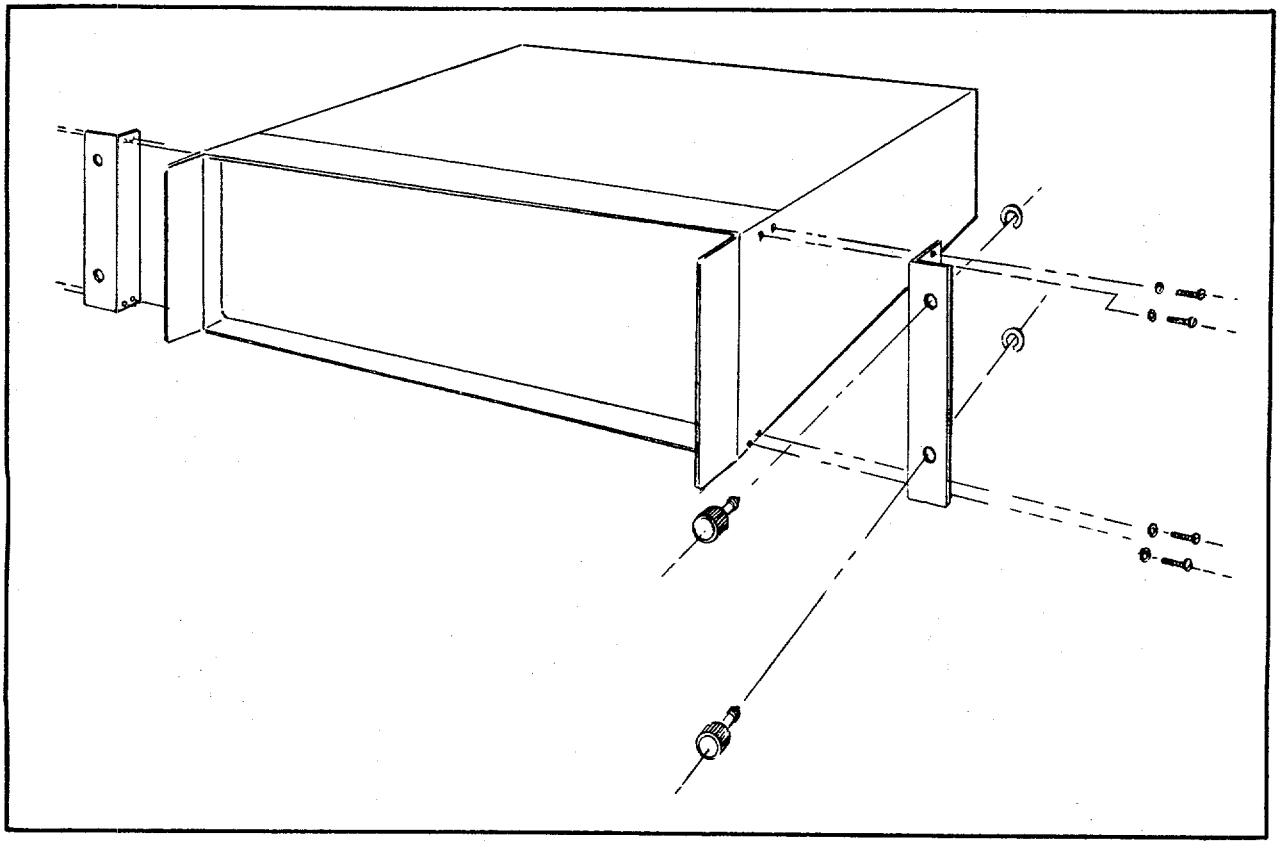


Figure 1-3. Rack Mounting Adapter Kit, Model 74124

SECTION II
INSTALLATION

2-1. GENERAL

After removal from the shipping carton, the Model 7413 Data Transmitter should be inspected for possible in-shipment damage. Report all damages in accordance with paragraph 1-3 of this part.

2-2. UNPACKING

The Data Transmitter is shipped in a reinforced packing case designed to provide maximum protection during transport and handling. While no special instructions are required for unpacking, care should be exercised in unpacking to prevent damage to the transmitter. The transmitter should be checked carefully.

2-3. MECHANICAL INSTALLATION

The transmitter can be used as a desk-top package or rack mounted. If the unit is to be rack mounted an optional rack-mount adapter kit is avail able. If the rack-mount kit is used, install the mounting brackets as shown in figure 1-3.

2-4. ELECTRICAL INSTALLATION

Power connection is made on the rear of the unit. All other input and output connections are available either on the front panel or on a terminal strip on the rear of the unit. (See figures 1-1 and 2-1.)(See table 2-1).

Figure 2-1. Data Transmitter, Model 7413 (Rear View)

Table 2-1. Input and Output Connections Chart

INPUTS

J3 (Rear Panel BNC)	Sync Input
J2-6	75 Baud
J2-25	150 Baud
J2-8	300 Baud
J2-27	600 Baud
J2-10	1200 Baud
J2-29	2400 Baud
J2-12	4800 Baud
J2-31	9600 Baud
J2-14	Non-integer rates
J2-2	+10 volts
J2-16, -17	-10 volts
J2-4	Signal Grd.
J2-23	Signal Grd.
J2-19	Chassis Grd.
J2-37	Chassis Grd.

OUTPUTS

TB1-1	+10 volts
TB1-2	Mark
J1-Ring Frt. Panel	Mark
J1-Tip Frt. Panel	Tongue
TB1-3	Tongue
TB1-4	Space
TB1-5	-10 volts
TB1-6, 7, 8	Blanks
TB1-9	Ckt. Grd.
TB1-10	Chassis Grd.

2-5. MODULE DESIGNATIONS (See figure 2-2)

Modules may be mounted in either vertical or horizontal assemblies. In either case, the basic building block is a frame which accepts four 50 module connector boards. Boards are lettered A, B, C, etc. , omitting letters which might be confused with numbers.

Individual module connectors on the board are arranged in a black-and white checkerboard fashion so that module locations are clearly defined. The module location (connector) is identified by its row and column location on the board.

Numbers cast along the top and bottom edges of the frame identify module connector columns (1 through 10) of each board. Letters A through E, cast along the sides of the frame, identify the module connector rows. A module is identified by its board, column, and row position in that order. A3C, for example identifies a module location on board A, column 3, row C.

Individual pin numbers are not marked, but are assigned numbers 1 through 10. The two remaining pins are used as a test point and a component tie-point if desired.

Identification of a single pin, anywhere in the System, is provided by a series of numbers and letters consistent with the pin location, connector board and module connector row and column. For example: the numbers C10A5 indicates pin number 5 of module 10A (column 10, row A) on connector board C. Modules are keyed so they cannot be inserted upside down.

2-6. POWER DISTRIBUTION

Most modules use identical pins to accept power. These are pins 6, 7 and 8 for +10 volts, ground and -10 volts respectively. "Push-on" jumper strips are frequently used to distribute power along rows of modules. These are not designated by number but are illustrated in jumper assembly drawings.

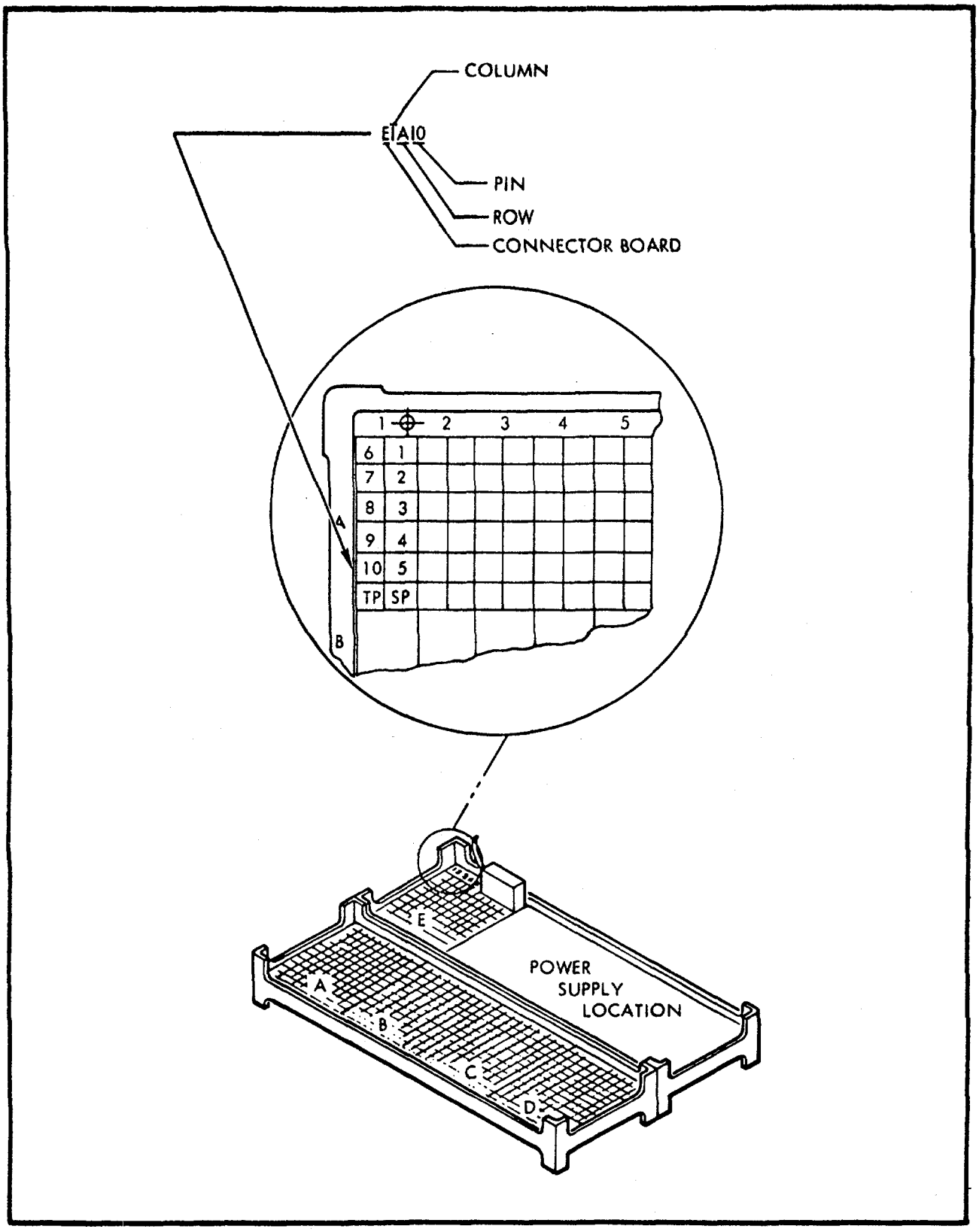


Figure 2-2. Reference Designations

SECTION III
OPERATION

CAUTION

Insertion of excessive dc voltages into the rear input connections (J2), due to improper connections at dc patch boards, will cause excessive damage to modules. Incorrect programming will also cause damage to modules.

3-1. GENERAL

The Data Transmitter, Model 7413, is designed to provide easy, reliable operation. All controls are quickly available to the operator, and are easily identified. (See Figures 3-1, 3-2 and 3-3 and Table 3-1).

3-2. CONTROLS AND INDICATORS

3-3. BAUD RATE (Rotary Switch)

Step 1. Set BAUD RATE switch to the desired rate position.

NOTE

The Transmitter BAUD RATE and Analyzer BAUD RATE switches must be set alike for baud rates that do not have a 2n x 75 baud relationship.

Step 2. Set RELEASE INFO switch to the desired operating mode. The operating modes are as follows:

(1) BIT SYNC

The data transmitter generates one bit of the character each time a trigger pulse is received at rear SYNC IN (BNC connect or). In the BIT SYNC mode, the BAUD RATE, internal STOP PULSE LENGTH, and BIAS DISTORTION switches are disabled.

Figure 3-1. Data Transmitter, Model 7413 (Front View)

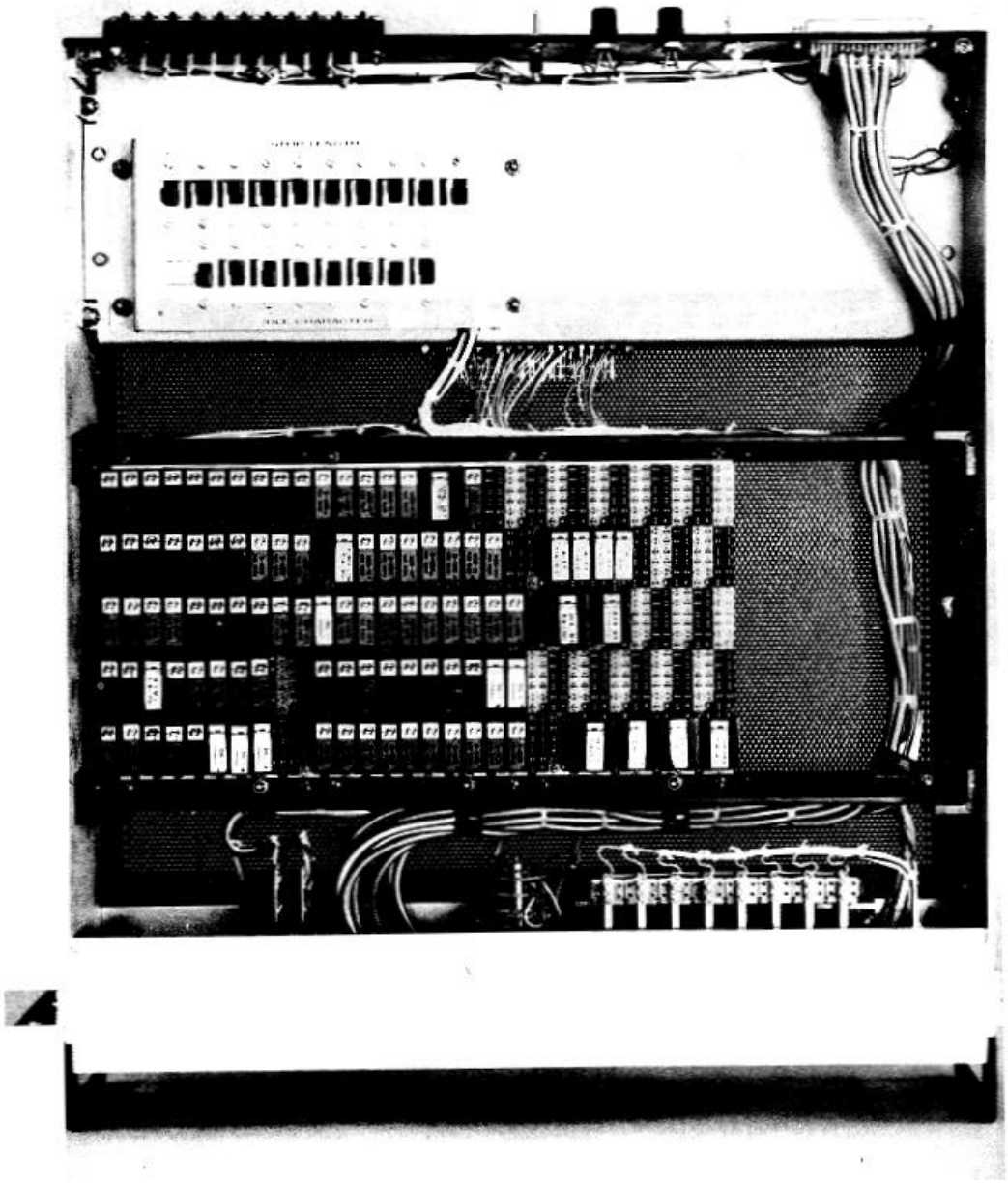


Figure 3-2. Data Transmitter, Model 7413 (Top View)

Figure 3-3. Data Transmitter, Model 7413 (Rear View)

Table 3-1. Controls and Indicators

Controls and Indicators	Fig. And Ref. No.	Function
PATTERN SELECTOR (Rotary Switch)	3-1	Selects four messages to be transmitted: 1. TEST MESSAGE 2. IDLE CHAR 3. SELECTED CHAR 4. REVERSALS
CODE LEVEL (Rotary Switch)	3-1	Selects the number of information bits per character to be transmitted and determines whether the transmitted characters will be STOP/ START or Synchronous.
RELEASE INFO (Rotary Switch)	3-1	Establishes the mode of operation of the unit.
STOP PULSE LENGTH (Internal Slide Switches)	3-1	Determines STOP PULSE length for STOP/START operation. The STOP PULSE length may be set in 0.01 unit increments from 1.00 to 2.00 units.
BAUD RATE (Rotary Switch)	3-1	Establishes the BAUD rate. Selects baud rate from the clock divider chain of the Analyzer.
POWER (Toggle Switch and Indicator)	3-1	Applies power to the unit and indicates power is being received from Analyzer.
PERCENT DISTORTION (Thumbwheel Switches)	3-1	The amount of distortion is controlled in 1% increments from 0% to 49%.

Table 3-1. Controls and Indicators (Cont'd)

Controls and Indicators	Fig. And Ref. No.	Function
BIT (IN-MARK OUT-SPACE) (Pushbuttons)	3-1	Character information content selected by these push buttons. The character is repeatedly generated by the transmitter when in selected CHAR mode.
SYNC POLARITY (Toggle Switch Rear Panel)	2-1	Determines whether information will be released on positive or negative transition of sync signal when operating in bit-sync mode.
SIG and SIG OUT (Indicator Lamp and Jack)		Indicator lamp is ON when a mark signal is generated and impedance across tip and ring of output jack is low.
BIAS DISTORTION (Rotary Switch)	3-1	Selects: ZERO MARKING SPACING SWITCHED type of distortion
IDLE CHAR (Internal Slide Switches)	3-1	Same as selected character but is programmed by internal slide switches.

(2) FREE RUN

In this mode of operation the transmitter continuously generates the selected format at the selected modulation rate.

(3) STEPPED

In this mode the transmitter generates one character of the selected format, at. the selected modulation rate, each time a trigger-pulse is received at SYNC in. If the trigger rate exceeds the character rate, which is deter mined by the BAUD RATE switch, the format will be transmitted at the character rate.

(4) STEADY MARK

In this mode the transmitter generates a continuous mark signal.

3-4. PATTERN SELECTOR (Rotary Switch)

Step 3. Set PATTERN SELECTOR switch

(1) REVERSALS

In this position the transmitter generates alternate marks and spaces at the selected bit rate. (The distortion controls do not function in this mode.)

(2) SELECTED CHARacter

The transmitter generates a single character repeatedly. The character information is selected by front-panel pushbutton switches.

(3) IDLE CHARacter

The transmitter generates a single character repeatedly. The information is selected by internal slide switches.

(4) TEST MESSAGE

The transmitter generates a standard message. The message content is programmed by a standard plug- in card.

3-5. CODE LEVEL (Rotary Switch)

Step 4. Set CODE LEVEL switch

This switch selects the number of information bits per-character to be transmitted, and determines whether the transmitted character is STOP/START or SYNC.

3-6. BIAS DISTORTION (Rotary Switch)

Step 5. Set BIAS DISTORTION switch

This switch selects the type of distortion desired, as follows:

ZERO:	Perfect Data (Percent distortion switches listed in paragraph 3-7 below do not function)
MARKING:	Marking bias distortion
SPACING:	Spacing bias distortion
SWITCHED:	In SWITCHED distortion, the type of distortion is switched automatically with each character transmitted; alternating marking bias or spacing bias distortion.

3-7. PERCENT DISTORTION (Thumbwheel switches)

Step 6. Set PER CENT DISTORTION switches

Distortion is controlled in 1% increments from "zero" to 49%.

3-8. SYNC POLARITY (Toggle Switch)

Step 7. Set Sync POLARITY switch

This switch, located on the rear of the chassis, determines whether information is released on the positive or negative transition of the sync signal when operating in bit-sync or stepped mode.

SECTION IV

PRINCIPLES OF OPERATION

4-1. GENERAL

The Data Transmitter Block Diagram (figure 4-1) and Logic Diagram (figure 4-2) are used as references in the following discussions:

One-hundred times the selected baud rate is derived from the Analyzer (See Data Analyzer, Model 7422, Instruction Manual) and is selected by the BAUD RATE switch in the transmitter.

The output of the clock divider is fed to a 0-50-0 up-down counter which divides the clock rate by 100.

An output from this counter, which is equal to the bit rate, is fed to the character-length generator. The character-length generator generates a series of pulses. The number of pulses is determined by the setting of the CODE LEVEL switch. These pulses are used to advance the shift register to transfer information into the distortion control circuits. Here the information is distorted and fed to the output circuits.

Another pulse is generated by the character-length generator at the beginning of the last bit. This pulse is used to transfer information from the format, or repetitive character circuits, into the shift register, and to advance the format sequencer to the next state. The input to the shift register from the selected format may be up to 8 lines, depending on the code level.

The shift register is a parallel-to-serial converter. Data is transferred into the shift register in parallel during the last

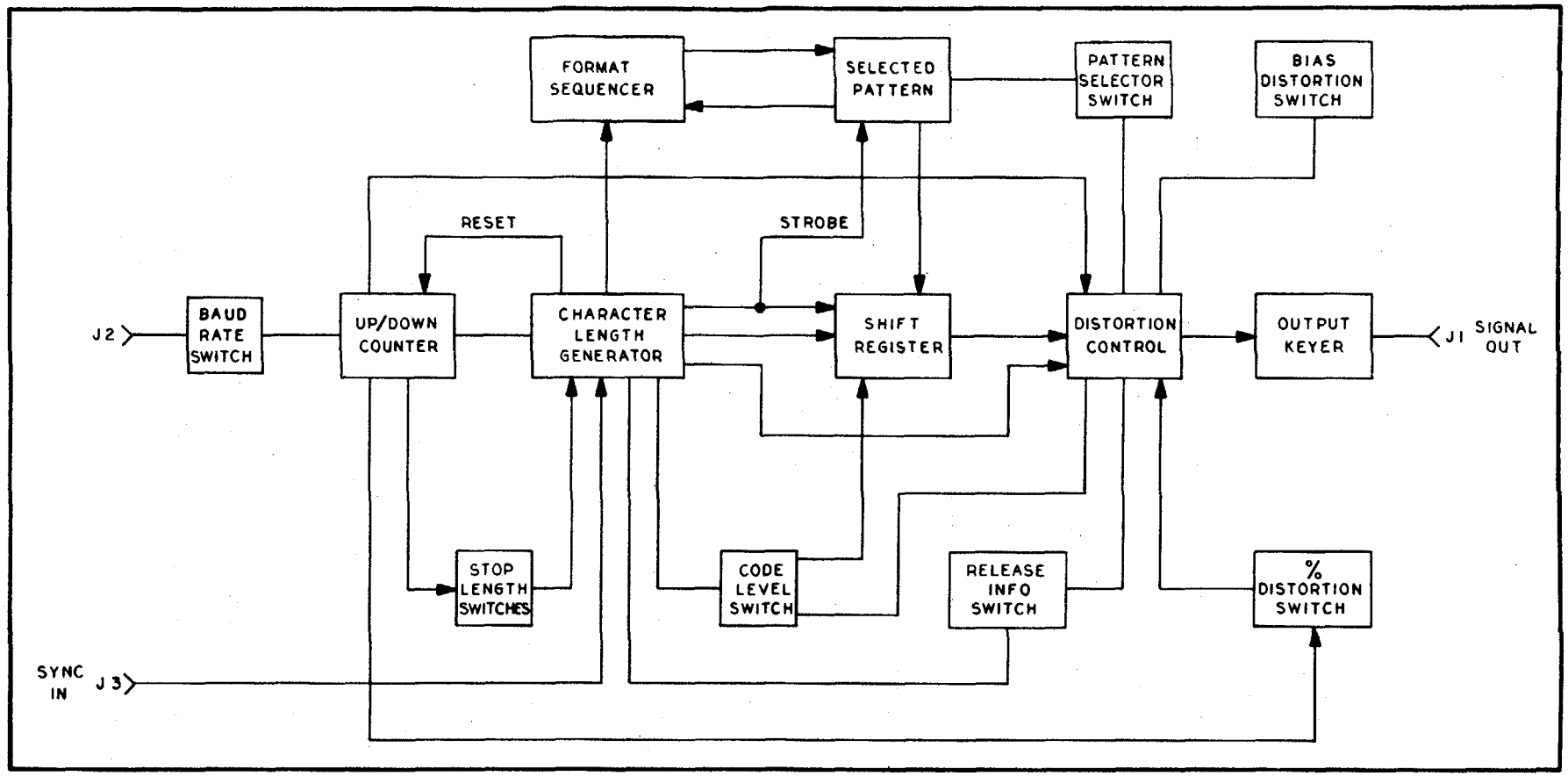


Figure 4-1. Data Transmitter, Block Diagram

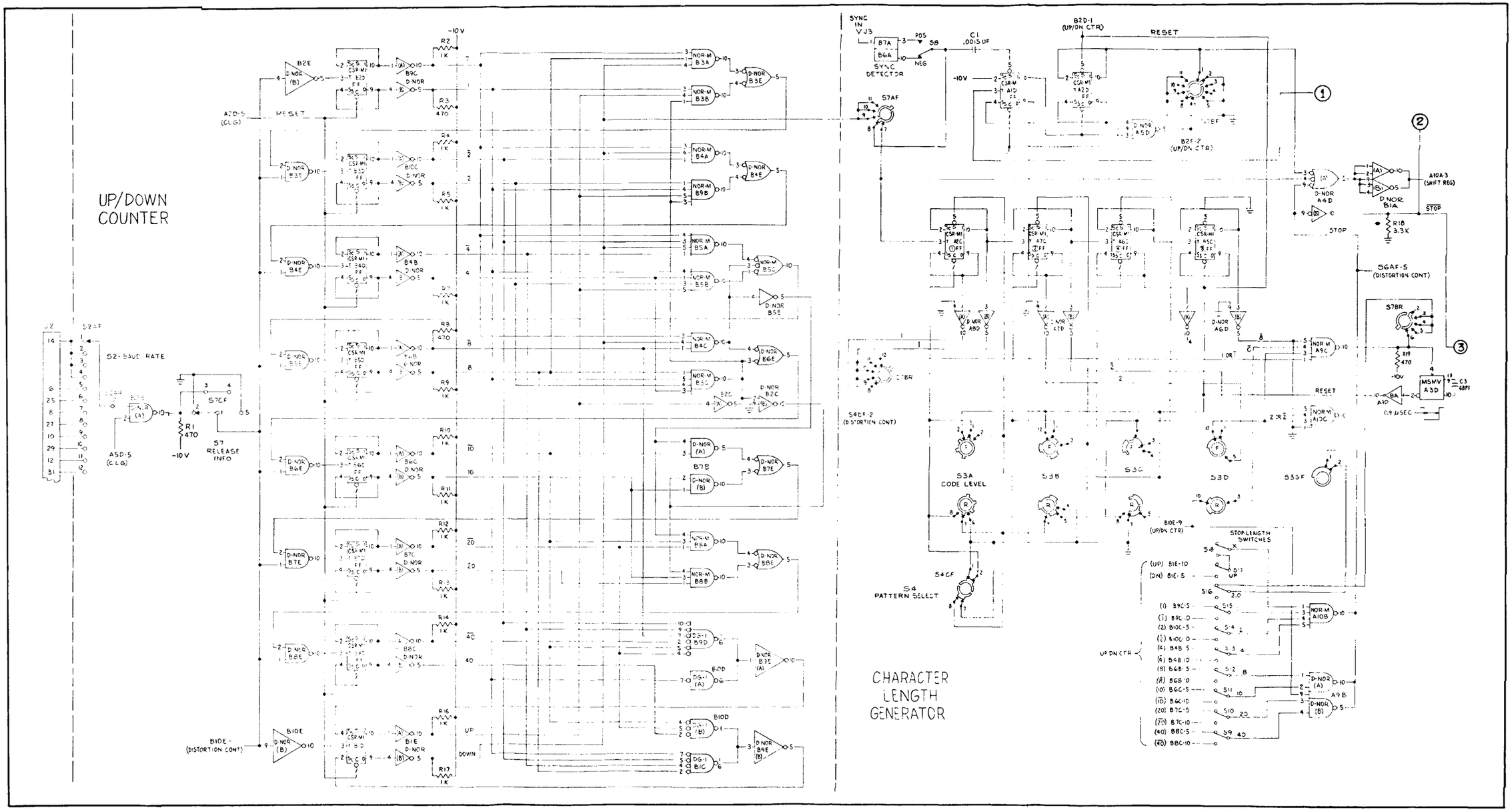


Figure 4-2. Data Transmitter, Logic Diagram G1, G2, and G3 Assembly (Sheet 1 of 4).

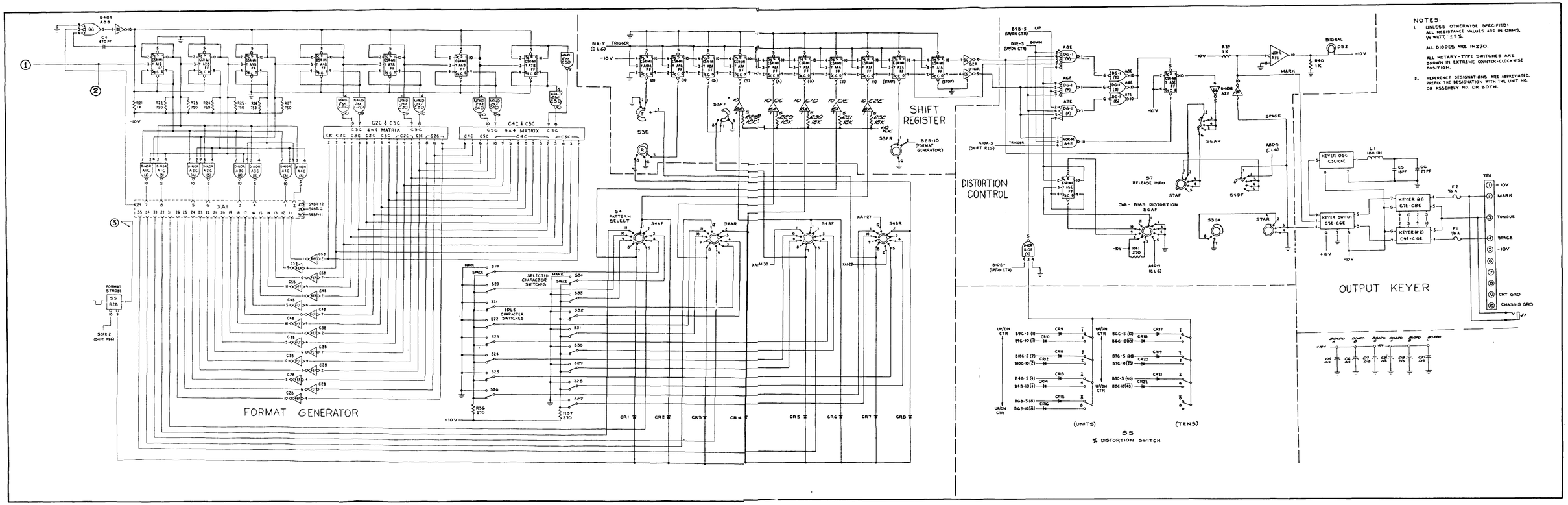


Figure 4-2A. Data Transmitter, Logic Diagram G1 Assembly (Sheet 2 of 4).

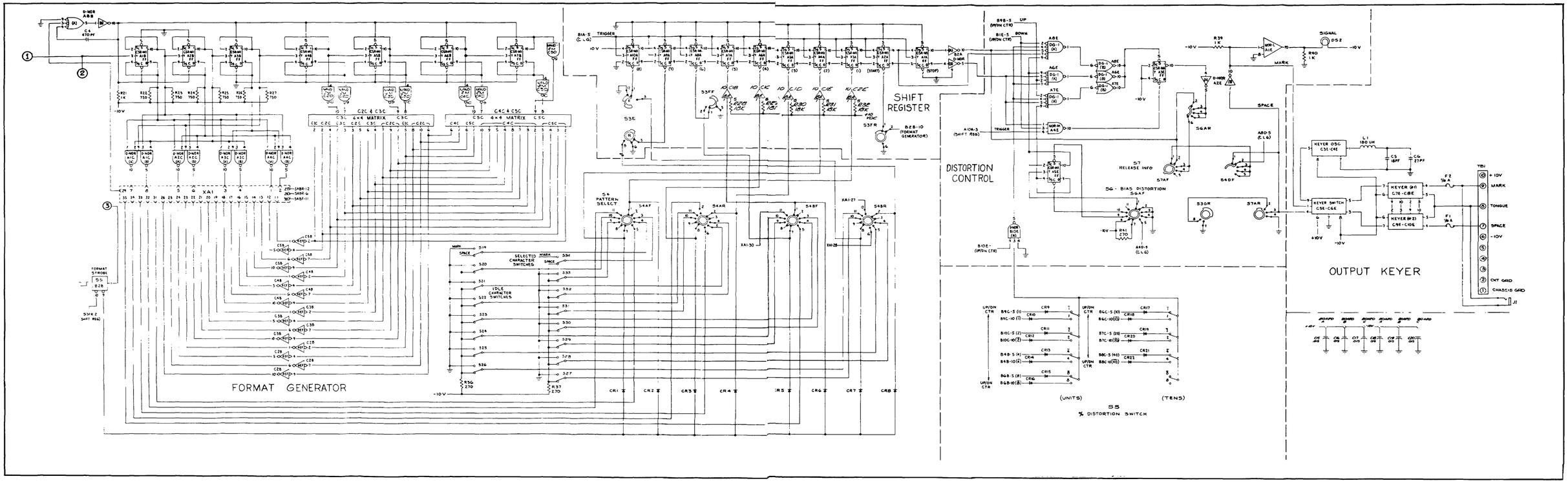


Figure 4-2B. Data Transmitter, Logic Diagram, G2 Assembly (Sheet 3 of 4).

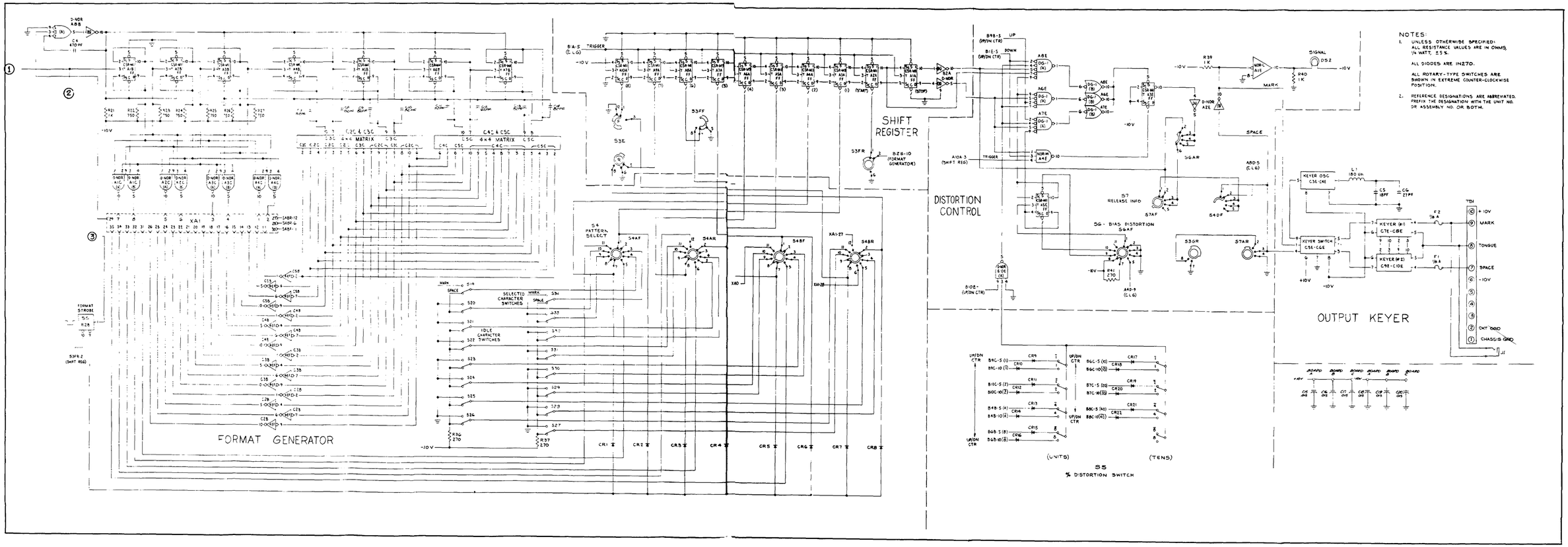


Figure 4-2C. Data Transmitter, Logic Diagram G3 Assembly (Sheet 4 of 4)

bit of the character, and is shifted out to the distortion control, serially, by the pulses from the character-length generator, during the next character interval.

The distortion control circuitry selects the type and amount of distortion and distorts the data from the shift register. The distorted signal then drives the output circuits.

In the STEPPED mode of operation, the input of clock pulses to the up-down counter is controlled by the sync signal at SYNC in. During the STOP pulse the clock signal is inhibited so that the output is left in a mark condition until the next external clock pulse.

In the BIT SYNC mode of operation, the timing of the character length generator is controlled by the sync signal at SYNC in. Thus, one shift pulse is fed to the shift register for each sync pulse at SYNC in. The STOP-pulse-length control and distortion control are by-passed, so the information output is dependent solely on the sync input rate.

4-2. DETAILED CIRCUIT DISCUSSION

Many of the circuits in the Data Transmitter are conventional logic circuits. The inter-connection of these circuits, and the operation of unique circuits, will be explained in detail. Logic symbols used are in accordance with MIL-STD-806B.

4-3. LOGIC ELEMENT AND APPLICATIONS IN DATA TRANSMITTER

Five types of logic modules are used in the Data Transmitters. These modules are described in the following paragraphs and illustrations:

4-4. Counter Shift Register, Medium Speed (CSR-MI)

The CSR-MI (Medium Speed) Counter Shift Register schematic, and an explanation of its operation, are detailed in figure 4-3.

4-5. Dual NOR, Medium Speed

The Dual-NOR (Medium Speed) schematic, and an explanation of its operation, are shown in figure 4-4.

4-6. NOR, Medium-Speed

The NOR (Medium Speed) schematic, and an explanation of its operation, are shown in figure 4-5.

4-7. Diode Gate (DG-I)

The Diode Gate schematic, and an explanation of its operation, are shown in figure 4-6.

4-8. NOR, Low Speed

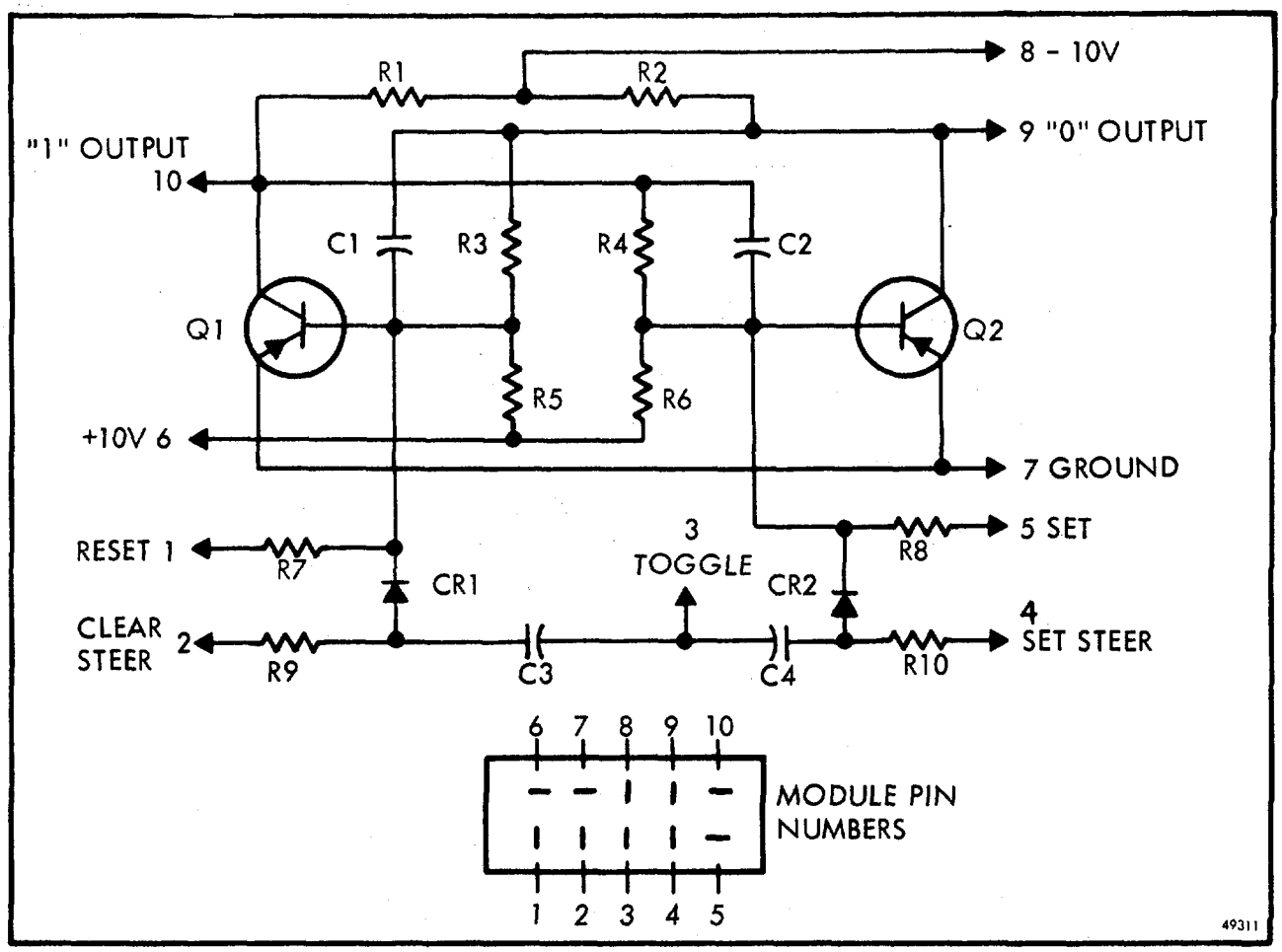
The NOR (Low Speed) schematic, and an explanation of its operation, are shown in figure 4-7.

4-9. NOR-Gate Application

The NOR-gate used in the Data Transmitter is a standard medium-speed resistor-transistor NOR. If all inputs are at ground the transistor is turned OFF, and the output is at -5 to -10 volts, depending on loading. If any input goes to approximately -5 volts, the transistor saturates and the out- put goes to ground.

4-10. Inverter (NOR-M) Application

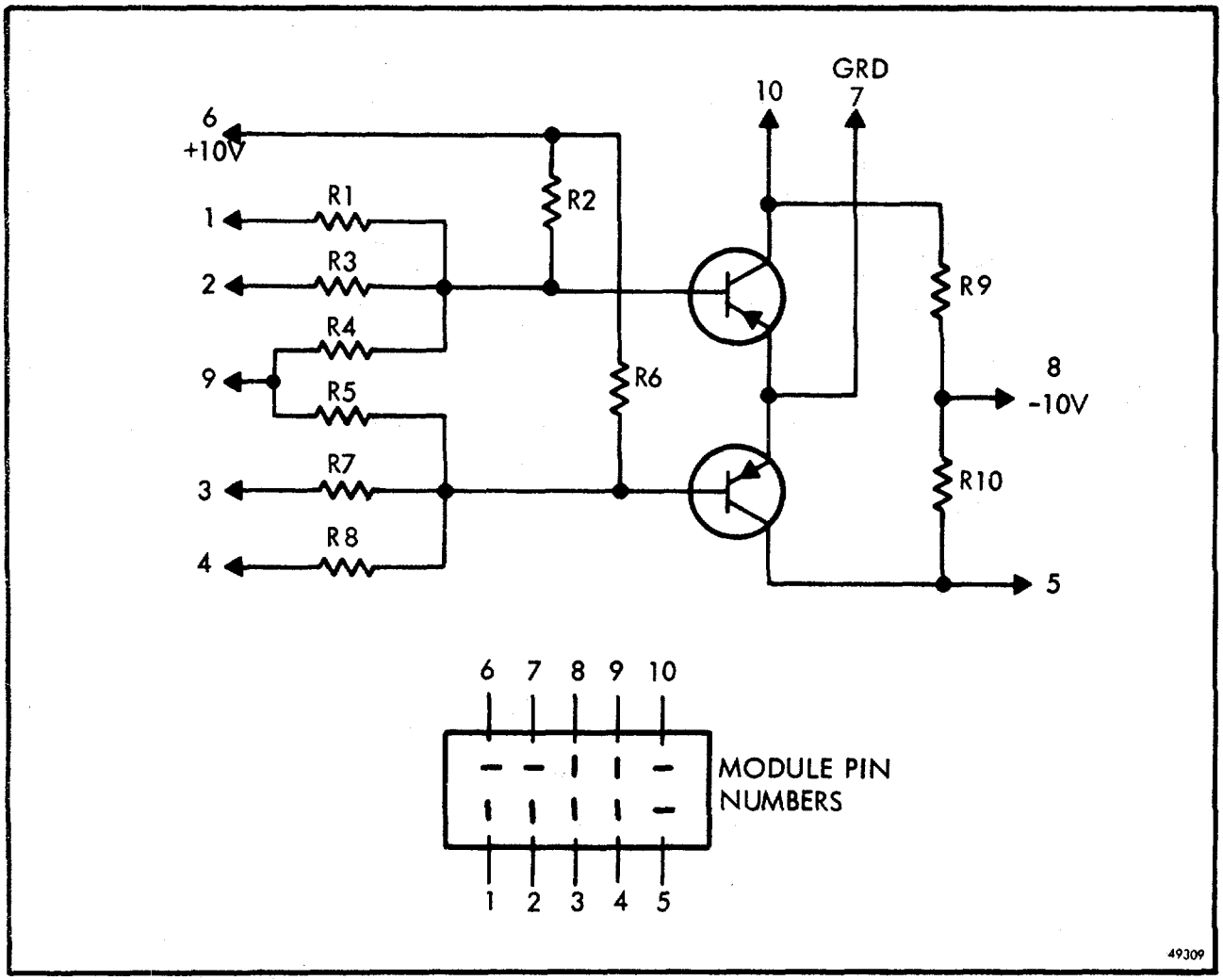
The circuit used in the Data Transmitter, for inverter and/or buffer applications, is a single-input NOR, identical to



A single CSR module is required to form a complete counter shift register circuit. The circuit output levels may be switched by either the DC SET and CLEAR inputs or by the STEER and TRIGGER inputs.

Switching of the CSR occurs only when the trigger input makes a positive transition and the DC set and clear inputs are at ground voltage level. If one steer input is at ground voltage level and the other is more negative than -5 volts, the CSR circuit outputs assume the same logic levels that the corresponding inputs had at the time of switching, the "'1" output being equal to the steer set (Ss) and the "0" output being equal to the steer clear (Sc) input. If both steer inputs are negative when the trigger input makes a positive transition, no switching occurs. If both steer inputs are at ground level when the trigger makes a positive transition, the operation of the circuit is undefined. Shift registers are formed by connecting "I" output of the CSR circuit to Ss input of the next stage and the ' I'"0 output to the Sc input of the next stage. Counters are formed by connecting the "'1" output of each stage to the trigger input of the next stage. In each stage the "1"' output is connected to the Sc input and the "O" output to the Ss input of the same stage. These connections are not shown on the logic diagrams in the interest of simplification.

Figure 4-3. Counter Shift Register (CSR-M1)

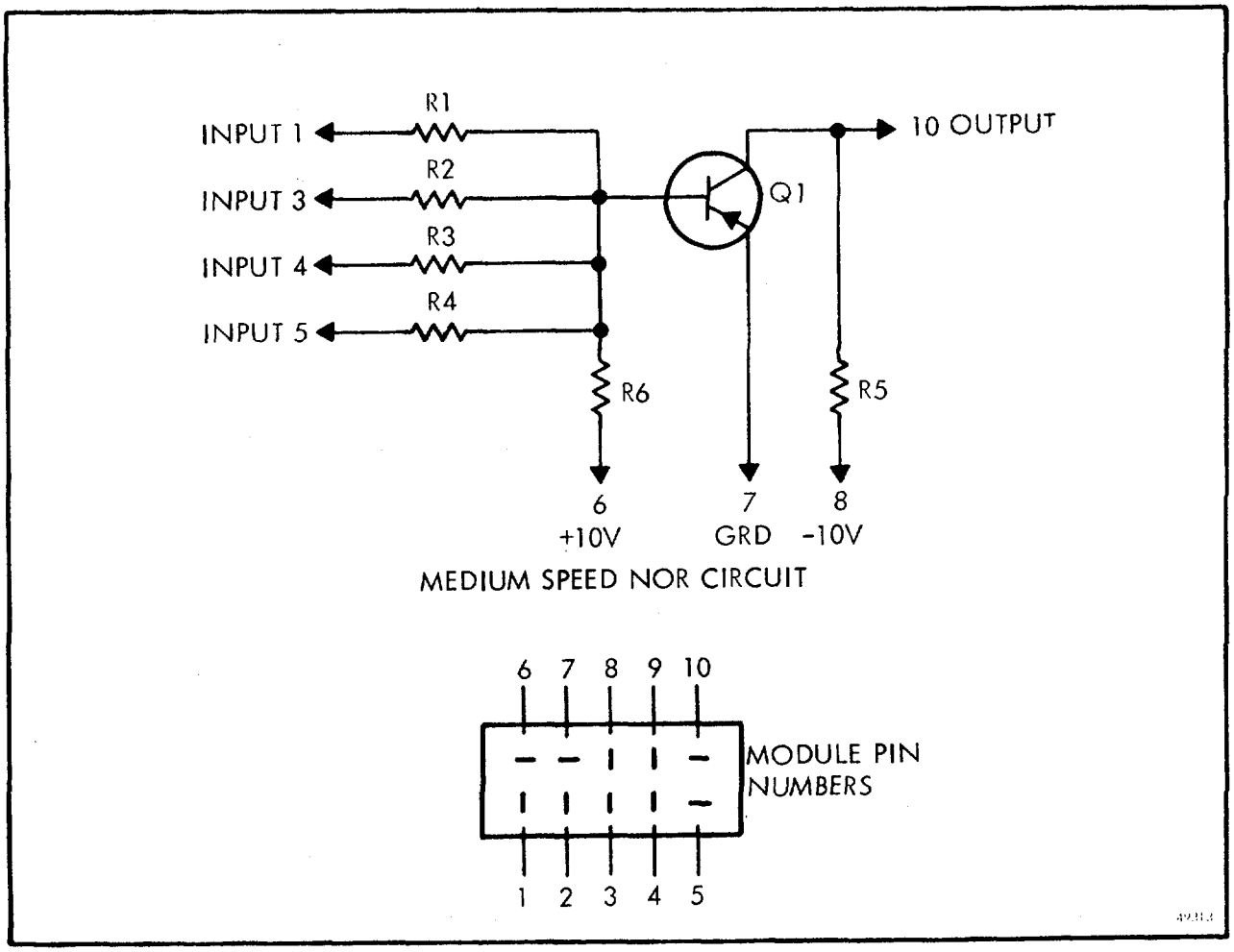


The Dual-NOR consists of two three-input logic NOR's within one module. Each NOR has separate inputs and one shared input.

The output at pin 10 will be 0.0 to -0.2 volts if inputs 1 or 2 or 9 are more negative than -5.7 volts. The output at pin 10 will be -5 to -10 volts (depending on the loading), if inputs 1, 2 and 9 ore all more positive than -0.2 volts. (An open input has the same effect as a grounded input.)

The output at pin 5 will be 0.0 to -0.2 volts if input 3 or 5 or 9 is more negative than -5.7 volts. The output at pin 5 will be -5 to -10 volts if inputs 3, 4 and 9 are all more positive than -0.2 volts.

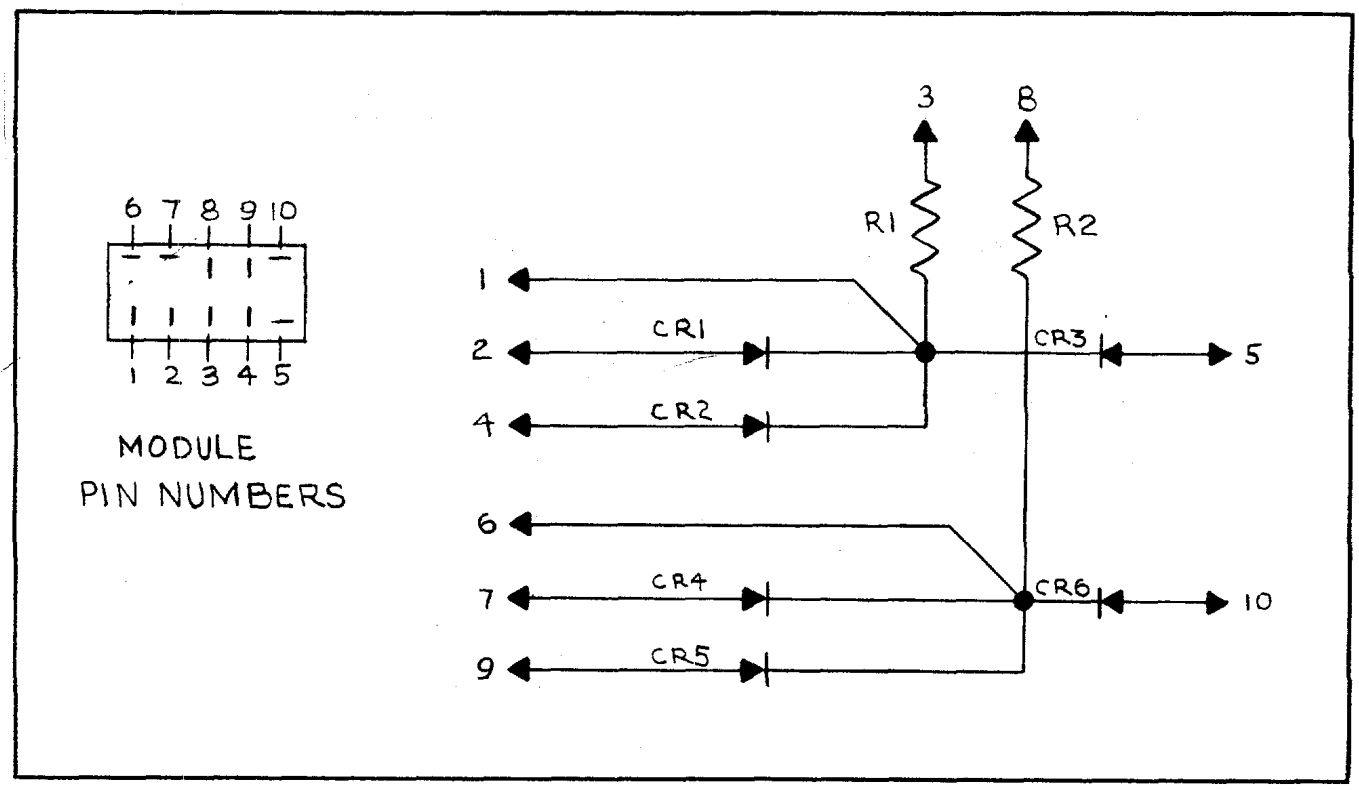
Figure 4-4. Dual - NOR, Medium Speed



The operation of a NOR module is such that if one input is more negative than -5.65 volts and the other three inputs are at ground or any negative voltage level the transistor is saturated. Under these conditions the output voltage is between 0 and -0.2 volt. If all four inputs are connected to the outputs of saturated transistors, the gating transistor is turned off, producing a nominal unloaded output of -10 volts. Connection of the maximum loads can decrease the negative amplitude to approximately -5 volts.

The operation of the NOR gate enables the performance of both the logical AND and OR functions with a single circuit. It inverts the logic levels in both cases. For negative-true inputs (logic "one" corresponding to -5 volts), the circuit performs the OR-NOT function $\overline{F} = A + B$. For positive-true logic (logic "one" corresponding to 0 volt), the circuit performs the AND-NOT function $\overline{F} = AB$. Therefore, all combination gating functions may be performed with the NOR circuit by using positive-true logic to perform AND functions and negative true inputs to perform OR functions.

Figure 4-5. NOR, Medium-Speed

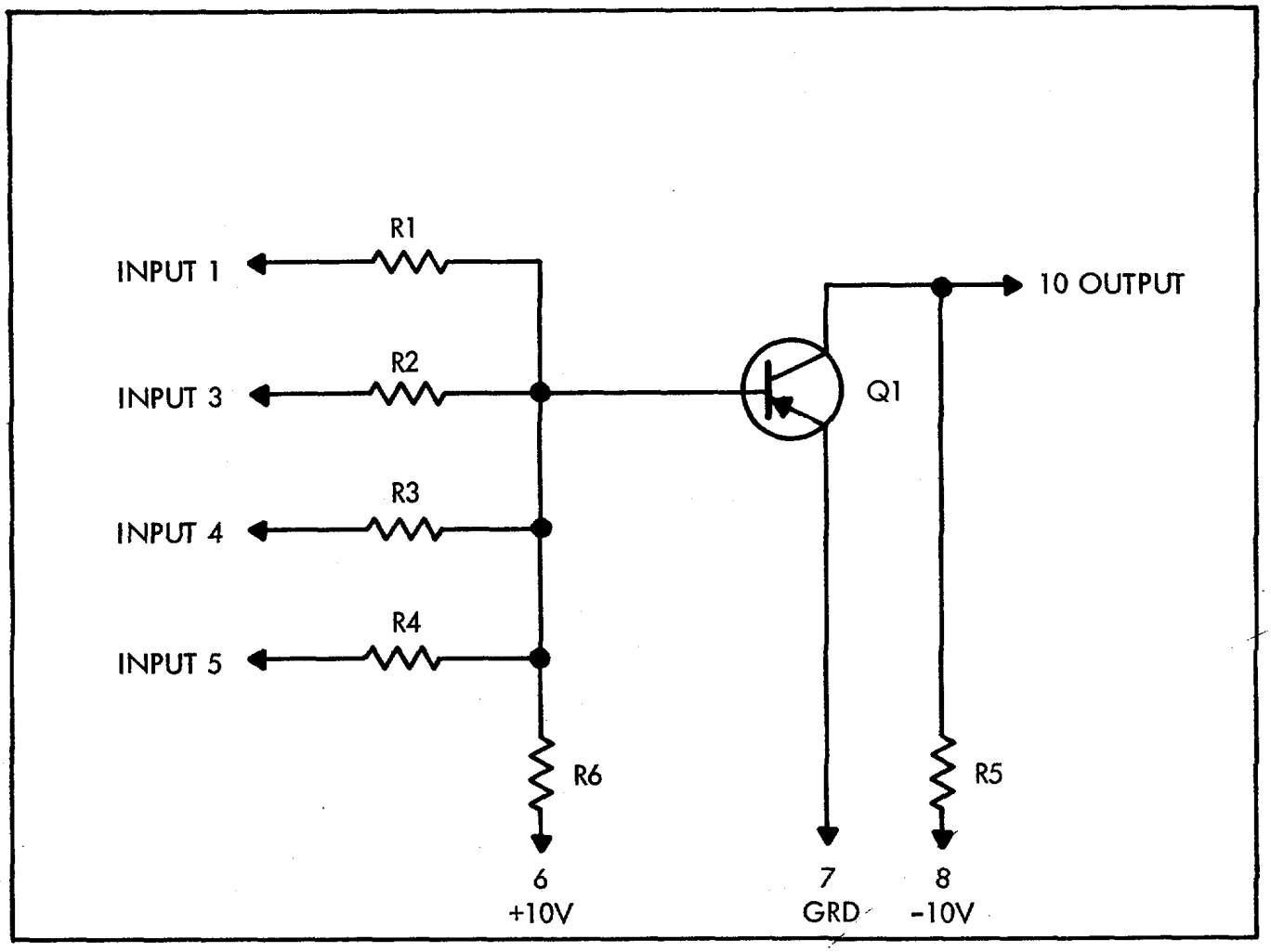


Two three-input negative coincidence diode gates are contained in one module when pins 3 and 8 are returned to -10 volts.

An exclusive OR may be formed using this module when pins 5 and 10 are externally tied together and biased with 8.2K ohm resistor to +10 volts (output at pins 5 and 10).

This module may be used with other standard modules but each application should be individually evaluated.

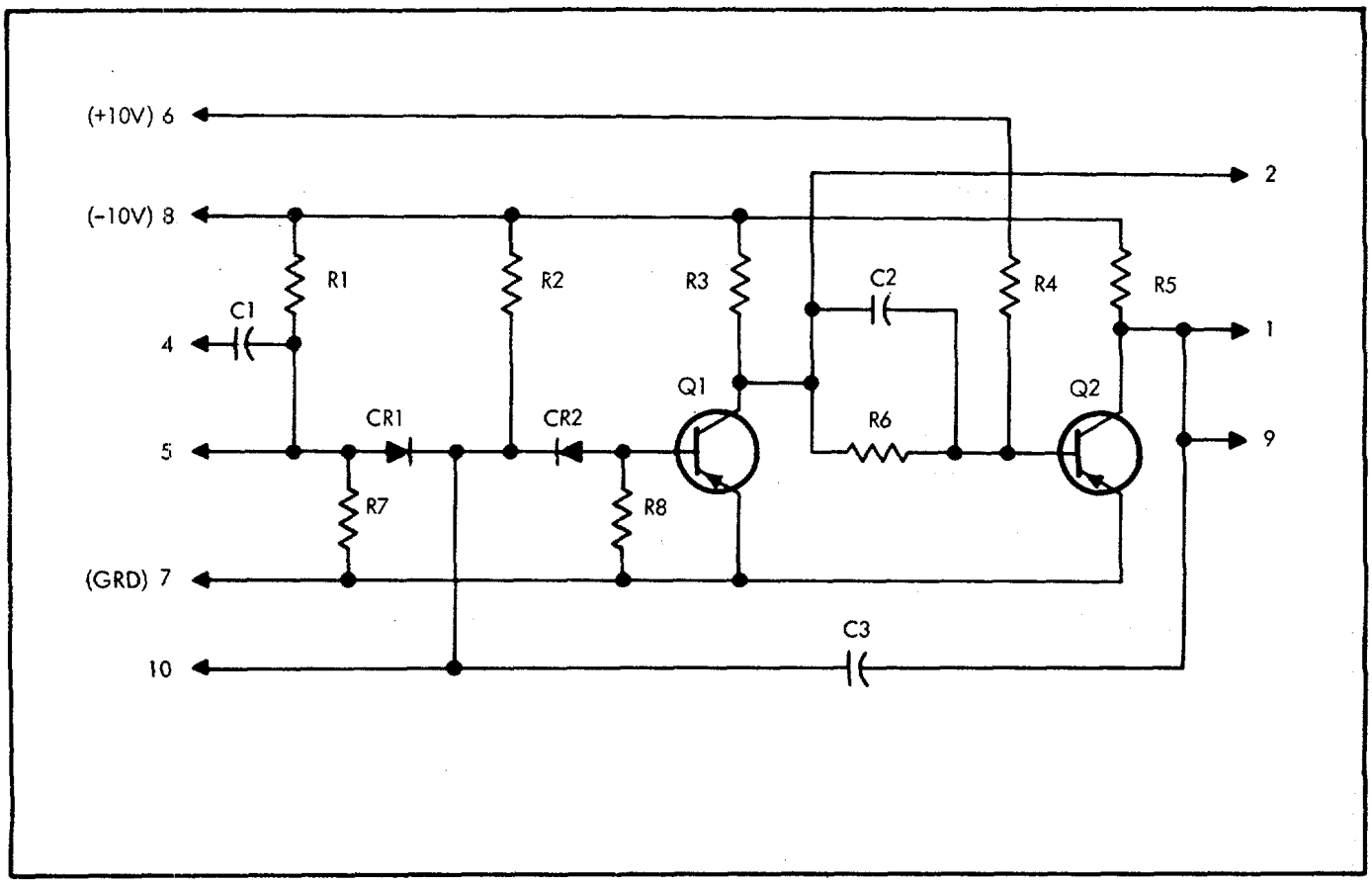
Figure 4-6. Diode Gate



The operation of a NOR module is such that if one input is more negative than -5.47 volts and the other three inputs are at ground, or any negative voltage level, the transistor is saturated. Under these conditions the output voltage is between 0 and -0.2 volt. If all four inputs are connected to the outputs of saturated transistors, the gating transistor is turned off, producing a nominal unloaded output of -10 volts.

The operation of the NOR gate enables the performance of both the logical AND and OR functions with a single circuit. It inverts the logic levels in both cases. For negative-true inputs (logic "one" corresponding to -5 volts), the circuit performs the OR-NOT function $\overline{F} = A + B$. For positive-true logic (logic "one" corresponding to 0 volt), the circuit performs the AND-NOT function $\overline{F} = AB$. Therefore, all combination gating functions may be performed with the NOR circuit by using positive-true logic to perform AND functions and negative-true inputs to perform OR functions.

Figure 4-7. NOR, Low-Speed



The MSMV circuit used in the transmitter operates on a positive-going transition at the input. The input pulse is differentiated by the input capacitor and the 3.3K (R1) and 1K (R3) ohms resistors. This positive spike then turns OFF the first transistor, causing its collector to go negative and turn ON the second transistor. Timing capacitor C, charges through 12K (R2) resistor, holding the first transistor cut-off until its charge reaches a negative level sufficient to cause the transistor to conduct. (See A3D, Figure 4-10)

Figure 4-7A. MSMV

the NOR-gate described above, except for the number of inputs.

4-11. INPUT DETECTOR

The input detector (see figure 4-8) circuit performs the same function as a Schmitt Trigger. A sine-wave, or other input waveform, causes the output to turn ON as the input goes negative, and cause it to turn OFF as the input goes positive. Output switching is regenerative, and is not a function of the slope of the input signal.

4-12. TIMING SOURCE

The timing source is derived from the Data Analyzer. (For timing techniques, see Data Analyzer Handbook, Part B of this manual.)

4-13. 0-50-0 UP-DOWN COUNTER

The up-down counter is a seven-stage BCD counter with an extra BSMV which is used to change the direction of the count. (See figures 4-1 and 4-2). See figure 4-9 for timing diagram.

4-14. CHARACTER-LENGTH GENERATOR

The character-length generator consists of a four-stage binary counter, NOR stop-length decoder, and programmable reset circuitry. (See figure 4-10 for timing diagram.)

4-15. STOP/START, 8-LEVEL CODE, FREE RUN

In this mode of operation the character-length generator receives its trigger input from the up-down control line in the 0-50-0 counter. The up-down flip-flop operates at one cycle per bit, and this advances the character-length generator at the selected bit rate.

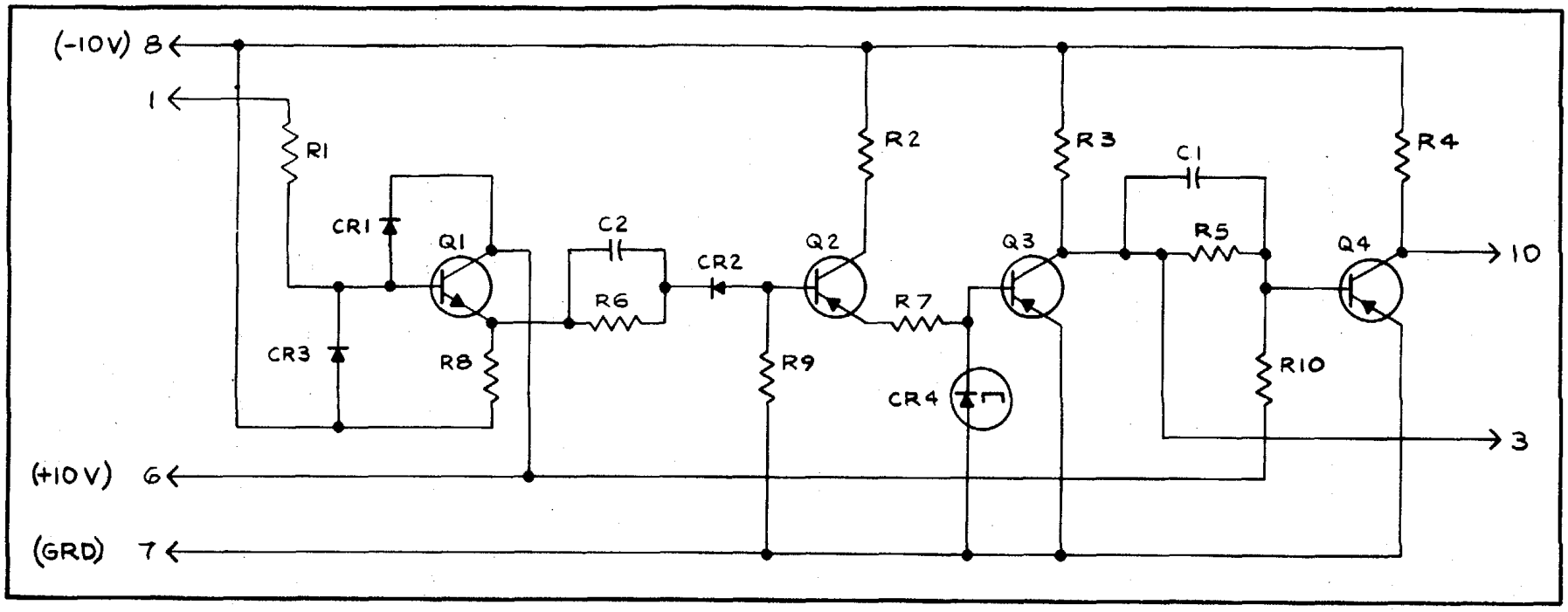


Figure 4-8. Sync Input Detector

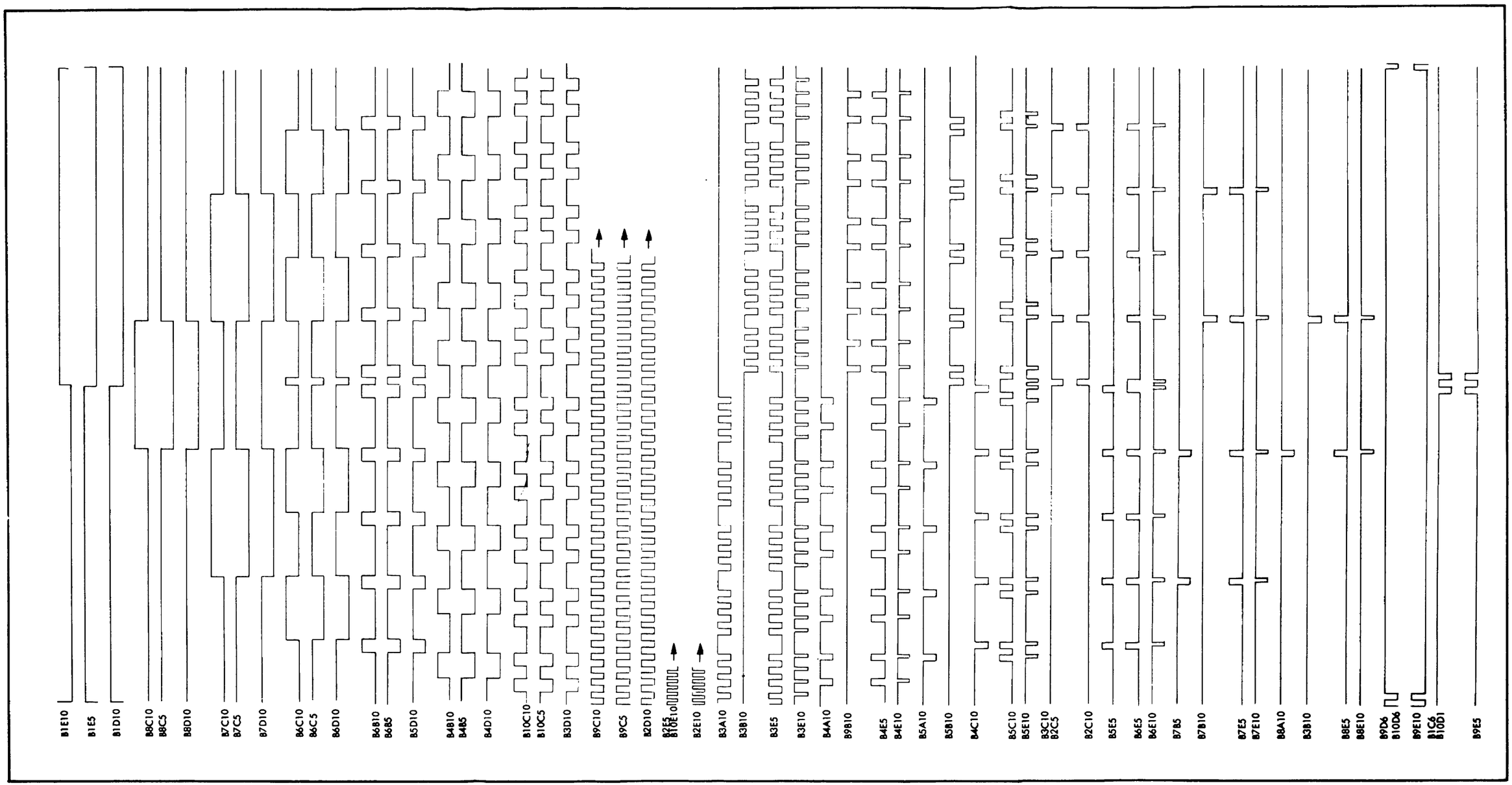


Figure 4-9. 0-50-0 Up-Down Counter, Timing Diagram

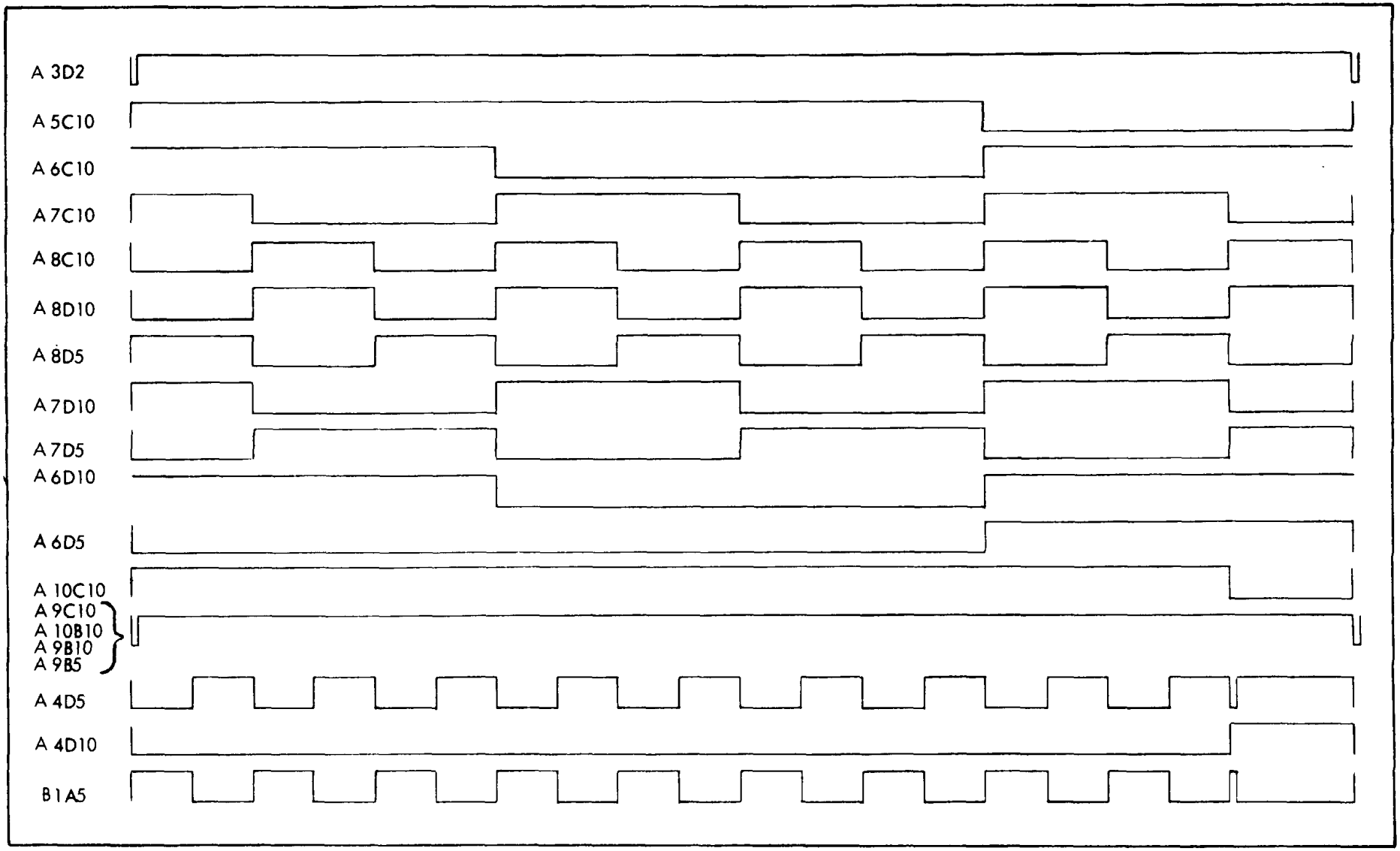


Figure 4-10. Character-Length Generator, Timing Diagram

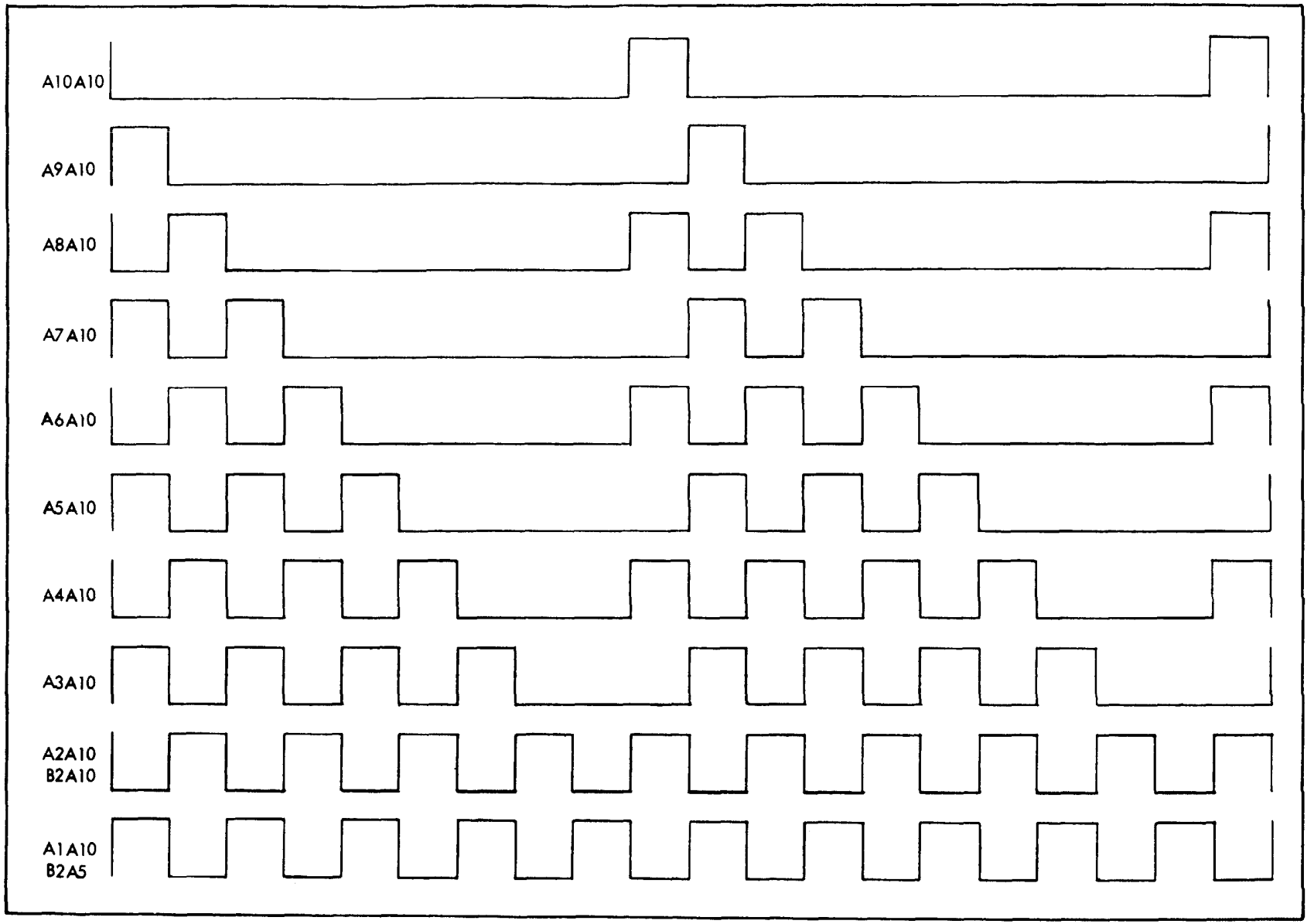


Figure 4-11. Shift Register, Timing Diagram. Stop/Start, 8-Level Code, Free Run, M-S-M-S-M-S-M-S

4-16. START/STOP (See figures 4-1 and 4-2)

The decoded counts of "10" and "11" are used for STOP pulse control. After the count reaches 10, the shift-register trigger pulses are inhibited by the shift-register gate (A4D). At the leading edge of the 10 count the format strobe generator is triggered and after a delay of approximately 0.2 usec, the format output is strobed into the shift register. Also at the count of 10 the format sequencer is advanced to the next character.

NOR-gates A10B and A9B determine STOP pulse length. The reset "one-shot" is fired by the positive-going trailing edge of the output from the above gates, and the character-length counter is reset. The 0-50-0 counter is reset to "0" by the same reset pulse. The next input pulse will occur at a one-bit interval after the STOP pulse.

When code-level 8 is selected, the reset pulse presets a count of 1 into the character-length counter. Two is preset for 7 level, 3 is pre set for 6 level, and 4 is preset for 5 level.

4-17. SYNCHRONOUS, 8-LEVEL CODE, FREE RUN (See figures 4-1 and 4-2)

In this mode of operation the STOP and START pulses are deleted from the transmitted character. This means that two shift pulses are deleted and the STOP length control is disabled. A count of 9 is used to reset the character length counter, provide the first shift pulse, and reset the 0-50-0 counter. When a count of 8 is reached, the prior described strobing action is performed.

4-18. EXTERNAL CHARACTER CONTROL, 5 LEVEL, STOP/START (See figure 4-1 and 4-2)

In this mode the rate at which characters of information are transmitted depends on the rate of the input at SYNC IN. Prior to arrival of a pulse at the SYNC IN input B7A1, the input to the clock inhibit gate is held negative by the output from gate A5D (1/2 Dual-NOR). This negative voltage blocks the clock pulses at B2E and prevents the up-down counter from running. The inputs that cause A5D to be negative are the "'zero" output from the ready flip-flop and the "one" output from the step flip-flop. The step flip-flop is in a cleared condition and the ready flip flop is set.

This condition is the rest condition of the equipment in the transmitter, while waiting an input sync pulse.

When the input sync signal crosses zero in either direction the in put detector senses this condition and the inverter puts out a negative transition. The 1500 picofarad input differentiating capacitor to the set input of the step flip-flop differentiates the negative-going leading edge of this transition pulse, and the resulting differentiated step function sets the step flip-flop. The output of the "one" side of the step flip-flop performs two functions: (1) It clears the ready flip-flop, and (2) it acts as an inhibit input to gate A5D.

The "zero" output of the ready flip-flop also appears at this gate as a second input that serves to hold the output of this gate (A5D) at "zero" condition until the output of the system is in STOP pulse.

When the output of gate A5D goes from negative to ground it removes the inhibit input to the clock inhibit gate B2E, permitting the clock pulses to again start the up-down counter.

Each time the up-down counter reaches "zero" the character length counter is advanced one count. The character-length counter continues counting the number of times the up-down counter goes through its cycle until the required number of pulses for the 5-level code, selected in this example, is reached.

At this time the character-length circuits produce the STOP pulse. The STOP pulse, the output of gate A4D10, goes from "one" to "zero". (See figure 4-10) This pulse triggers the step flip-flop from the set to the cleared condition, removing the one negative input of gate A5D. How ever, this does not stop the up-down counter from running as the "zero" output from the ready flip-flop A2D (still in the cleared condition) holds A5D5 at ground.

At the completion of the STOP pulse the reset pulse acts as a set in put to the ready flip-flop which then goes to the "one" state. The zero output of this ready flip-flop provides "zero" input to gate A5D and the output of A5D goes to a "one" acting as an inhibit to clock-control gate B2E stop ping the counter. If the sync input rate is slower than the character rate for the selected baud rate, the output will rest in a mark condition awaiting the next sync pulse. It is necessary to provide this ready flip-flop to prevent

shortening the STOP pulse thereby permitting the stop pulse logic to generate the correct length of STOP pulse.

The "one" output of the ready flip-flop is also used to inhibit a shift register trigger during the STOP pulse in this stepped character mode of opera tion. If not inhibited, the shift register would advance into the next pulse which would be START, and it would rest in a START instead of a STOP mode.

4-19. BIT SYNCHRONOUS, 5-LEVEL, STOP/START (See figures 4-1 and 4-2)

In this mode, the release of information from the shift register is accomplished at the rate of one bit for each input pulse at SYNC in. The STOP length control, distortion control and internal bit rate generators are disabled. The character-length counter receives its trigger from the sync input.

The operation of the character-length generator circuitry is the same as described in paragraph 4-14, except for the source of trigger pulses. The counter operates at the rate of the sync input, and the shift register is triggered at the same rate.

4-20. STOP-PULSE LENGTH CONTROL

The STOP pulse length control circuitry decodes a number between 0 and 99 from the 0-50-0 counter, to be used in the character-length generator for determining the length of the STOP pulse. (See table 4-1 for STOP PULSE switch setting).

The output which is selected then represents 0.00 to 0.99 bits to be added to the end of the STOP pulse in the character-length generator.

Table 4-1.

Stop Pulse Switch Settings

Stop Pulse Length	Switch Positions									
	40	20	10	8	4	2	1	2.0	UP	X
1.00	0	0	0	0	0	0	0	0	0	0
1.42	1	0	0	0	0	1	0	0	1	1
1.50	1	0	1	0	0	0	0	0	0	0
1.75	0	1	0	0	1	0	1	0	0	1
1.99	0	0	0	0	0	0	1	0	0	1
2.00	0	0	0	0	0	0	0	1	0	0

The 1.00 and 2. 00 unit stop pulses are switch-selected as inputs to NOR modules A10B and A9B. These gates decode a number as shown in table 4-1 for the desired STOP pulse length.

As can be seen from the logic diagram (figure 4-2) for a 2.0 unit STOP pulse, A10B and A9B are disconnected and the STOP pulse will be two units wide. The STOP pulse length is terminated by the reset "one-shot" which is triggered by the positive-going transition of gate A9C. See figure 4-9 showing waveforms for representative switch settings and results.

4-21. FORMAT GENERATOR

This generator (see figures 4-1 and 4-2) makes use of timing signals from the character-length generator to initiate the message to be transmitted.

4-22. EIGHT-COUNTER AND MATRIX

The 8-counter is a simple 3-stage binary counter which drives an eight-line NOR decoder matrix. (See modules A1C through A4C on For mat Generator logic.) The selected output line for any given count is at a negative potential, while all other lines are at ground. The input to the 8 counter is derived from the STOP output of the character-length generator (A4D10). It advances one count per character.

4-23. SIXTEEN-COUNTER AND MATRIX

The 16-counter is a 4-stage binary counter which receives its trigger from the last stage of the 8-counter. This causes the 16 counter to advance once for each full count in the eight counter.

The decoding matrix consists of two modules and has 16 lines out, which drive 16 emitter-followers.

(See figure 4-13) The selected line for a given count is negative, while all other lines are at ground. The outputs of both matrices are ANDed in the format card to provide 128 lines.

4-24. FORMAT CARD (BAUDOT)

In the format card (figure 4-14) each line from the 16-matrix is terminated with eight resistors. Each of these is connected through a diode to one of the eight outputs from the 8-matrix. By this means only one of the 128 lines will be negative at any one time. Each of these 128 lines is fed into up to eight OR-gates, depending on the code selected. The outputs of these OR-gates are held at ground until the beginning of the STOP pulse, or last bit. At this time the eight outputs are released and the selected gates go to a negative potential. This information is read directly into the shift register.

At the end of the programmed message, a line may be used to advance the eight and 16-counters, to prevent a prolonged waiting period between messages. In this case, the line representing the next count may be connected to the "advance" output of the format card. This output triggers a dual-NOR module connected as an MSMV which advances the eight and 16-counters to a count of 124.

4-25. SELECTED CHARACTER

In this mode of operation, information is fed to the shift register from eight front-panel pushbutton switches. The method of strobing is the same as with the format card.

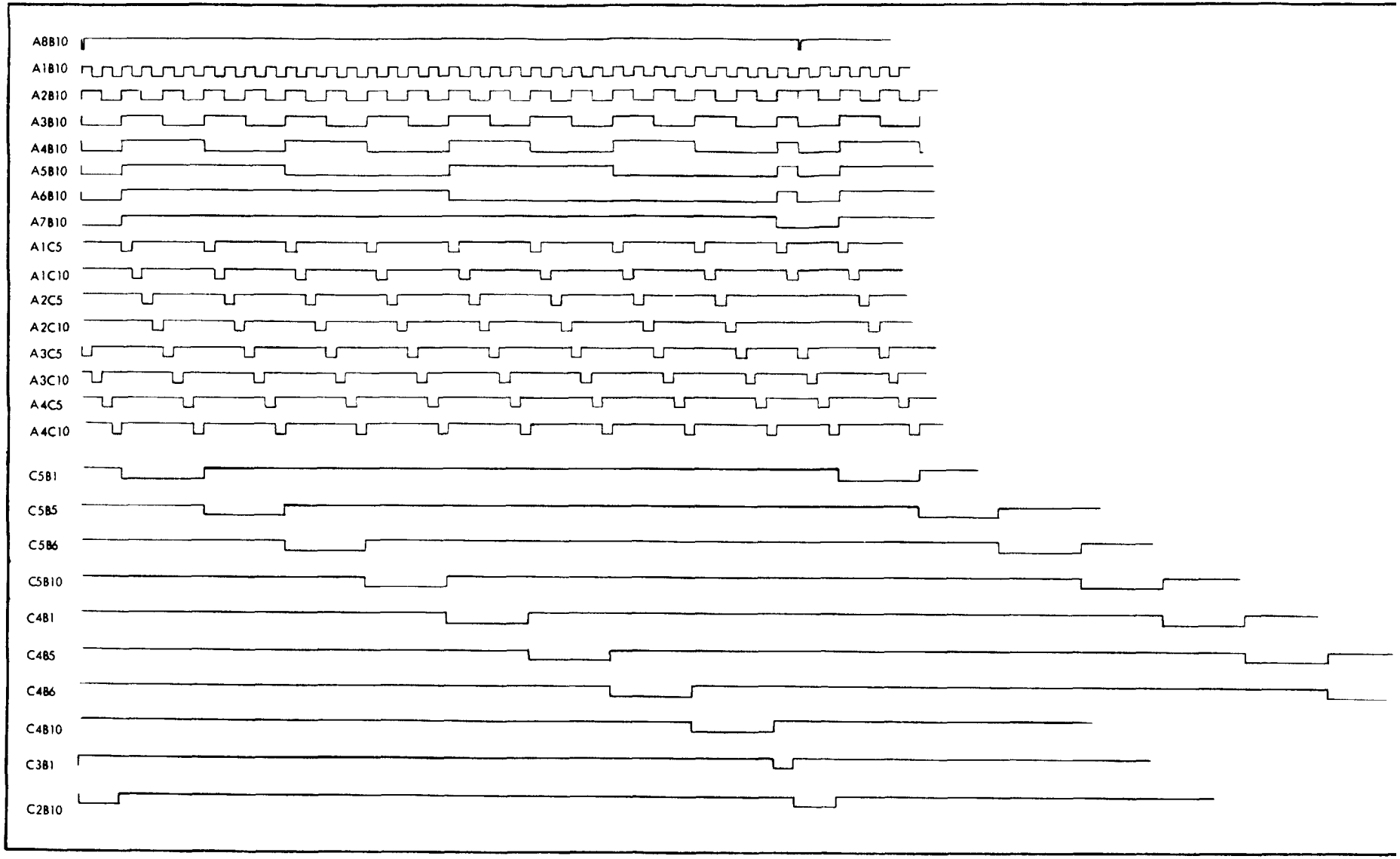


Figure 4-12. Format Generator, Timing Diagram

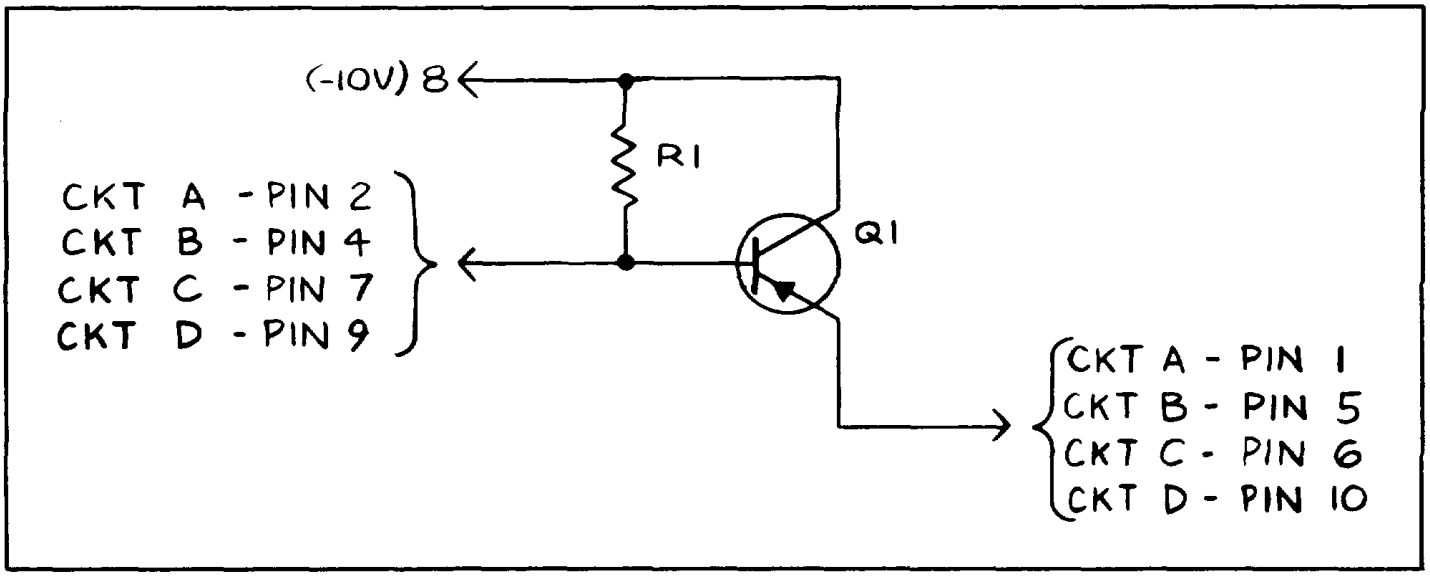


Figure 4-13. Emitter-Follower

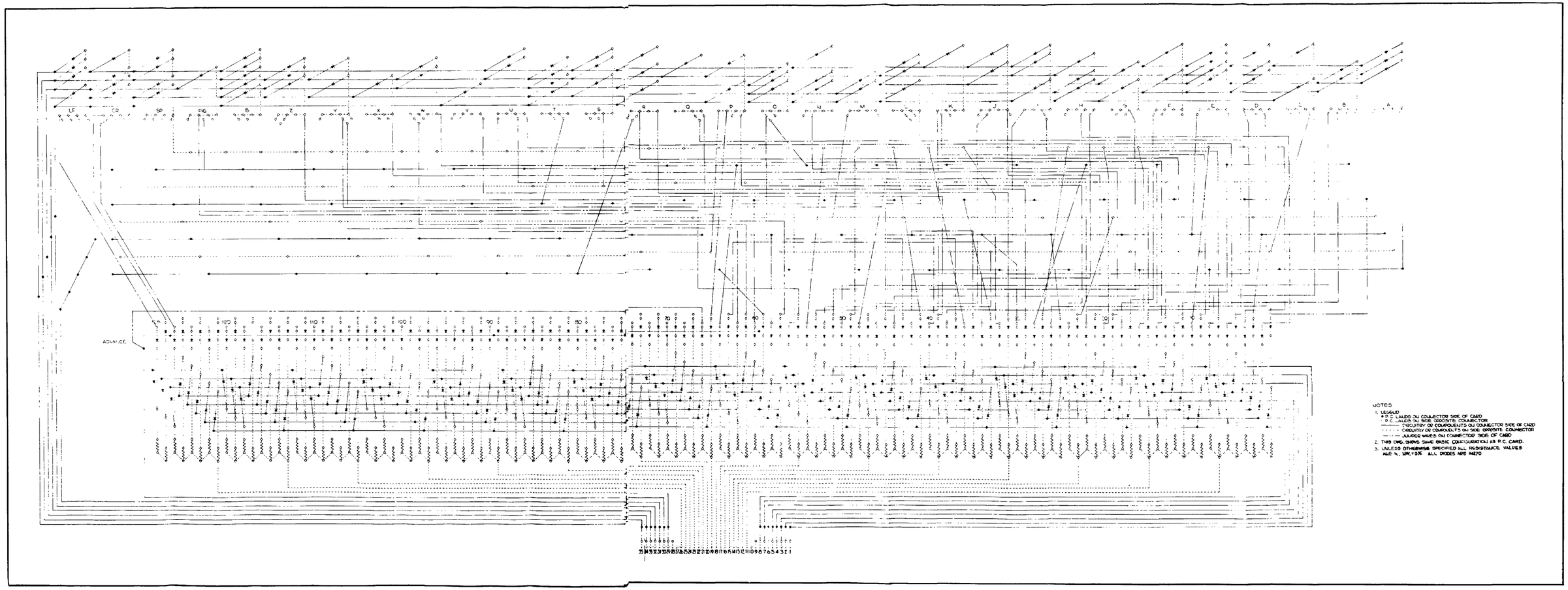


Figure 4-14. Baudot Format, Schematic Diagram

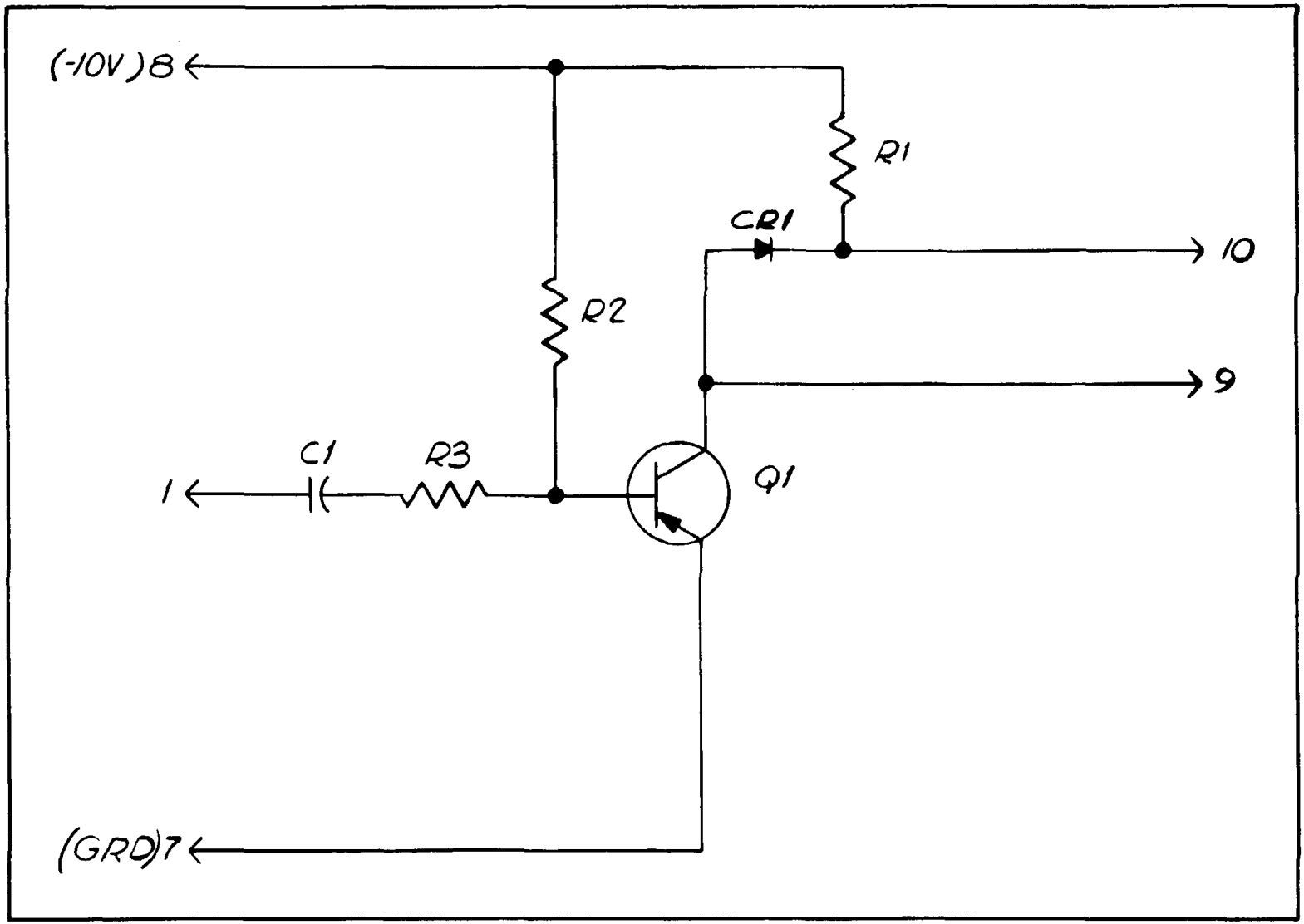


Figure 4-15. Format Strobe Circuit, Schematic Diagram

4-26. FORMAT STROBE

The format strobe circuit (figure 4-15) with a capacitor input from the STOP (A4D10) is in the character-length generator. The transistor is biased ON. When a positive transition occurs, the input capacitor differentiates the level change and the transistor is turned OFF for approximately 5 microseconds. The rise time and delay, through the input circuit, is sufficient to allow the 8-counter and 16-counter transitions to occur be fore any information is transferred. A negative transition has no effect on the strobe circuit.

4-27. SHIFT REGISTER

The shift register (shown in figures 4-1 and 4-2) is composed of ten standard CSR-M1 flip-flop stages, each one steered by the preceding stage. The first stage is steered by fixed levels so that it will always assume a "one" condition on the first shift pulse. Information is shifted, from left to right, by shift pulses formed in the character-length generator.

4-28. STOP/START

At the end of a series of shift pulses, all stages in the shift register will have assumed a "one" condition, corresponding to a mark in Baudot code. Information, representing spaces, is fed to the clear input of the CSR-M1 flip-flops from the format generator. The tenth CSR-M1 (counting from left to right) will always be left in a "one" condition, representing a STOP pulse. The ninth CSR-M1 is set to "zero" representing the START pulse.

As shift pulses are fed to the shift register, the data set into the preceding

stages appears at the last stage and is fed to the distortion control.

4-29. SYNCHRONOUS OPERATION

In synchronous mode, the operation of the shift register is similar to that in STOP/START mode, except that the ninth and tenth CSR-MI's store the last two bits of information. Data is strobed into the preceding stages at the time of the next-to-last shift pulse, and no clear pulse is sent to the ninth CSR-M1. This prevents the advancing "one" condition from reaching the ninth CSR-M1.

For code levels other than 8-bit, the clear inputs of the first three CSR-Ml's are grounded so that data may not be strobed into them.

4-30. DISTORTION CONTROL

The distortion control section (figures 4-1 and 4-2) consists of a mark-space-distort flip-flop CSR-M1 (A5E), distortion logic gating, PERCENT DISTORTION thumbwheel switches, flip-flop (A3E) and output dual-NOR buffers (A2E). (See figure 4-16 for timing diagram)

The mark-space-distort flip-flop determines the type of distortion to be generated. In the SWITCHED mode of operation, this flip-flop is toggled to provide alternate marking and spacing distortion.

The PERCENT DISTORTION thumbwheel switches decode a number between 0 and 49 from the 0-50-0 counter. This pulse determines the amount of distortion to be added to the signal. If the decoded number is used during the up count of the 0-50-0 counter, it creates spacing distortion. If it is used during the down count, it creates marking distortion.

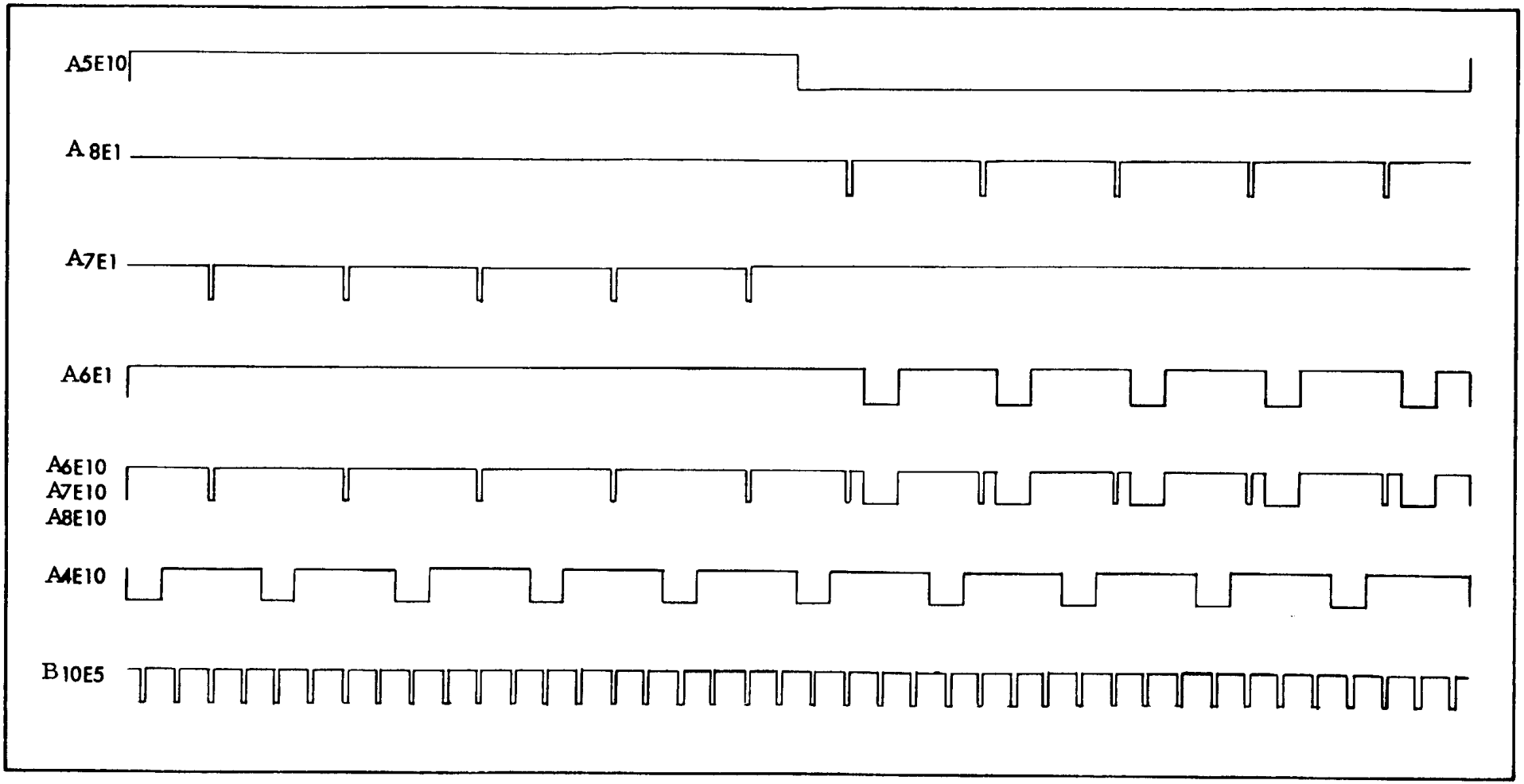


Figure 4-16. Distortion Control, Timing Diagram

4-31. MARKING DISTORTION

In marking distortion, flip-flop A3E is set earlier than an undistorted signal would occur, by the action of diode AND-gates A8E or A6E. The flip-flop is then cleared at the correct time by the action of NOR-gate A4E.

4-32. SPACING DISTORTION

In spacing distortion, flip-flop A3E is set later than an undistorted signal would occur, by the action of diode AND-gate A7E. Clearing takes place the same way as in marking distortion.

4-33. REVERSALS

In this mode of operation the output of the first counter stage in the character-length generator is connected directly to the output buffer in the distortion control section. This flip-flop goes through one half-cycle of operation during the period of one bit, yielding an output representing alternate marks and spaces at the selected bit rate.

4-34. CONTINUOUS MARK OR SPACE

For continuous space output the RELEASE INFO switch is set to FREE RUN, the PATTERN SELECTOR switch is set to SELECTED CHAR ACTER, the CODE LEVEL switch is set to 5 SYNC and all CHARACTER pushbuttons are OUT.

For continuous mark output, the input of the output buffer is connected directly to ground by the RELEASE INFO switch.

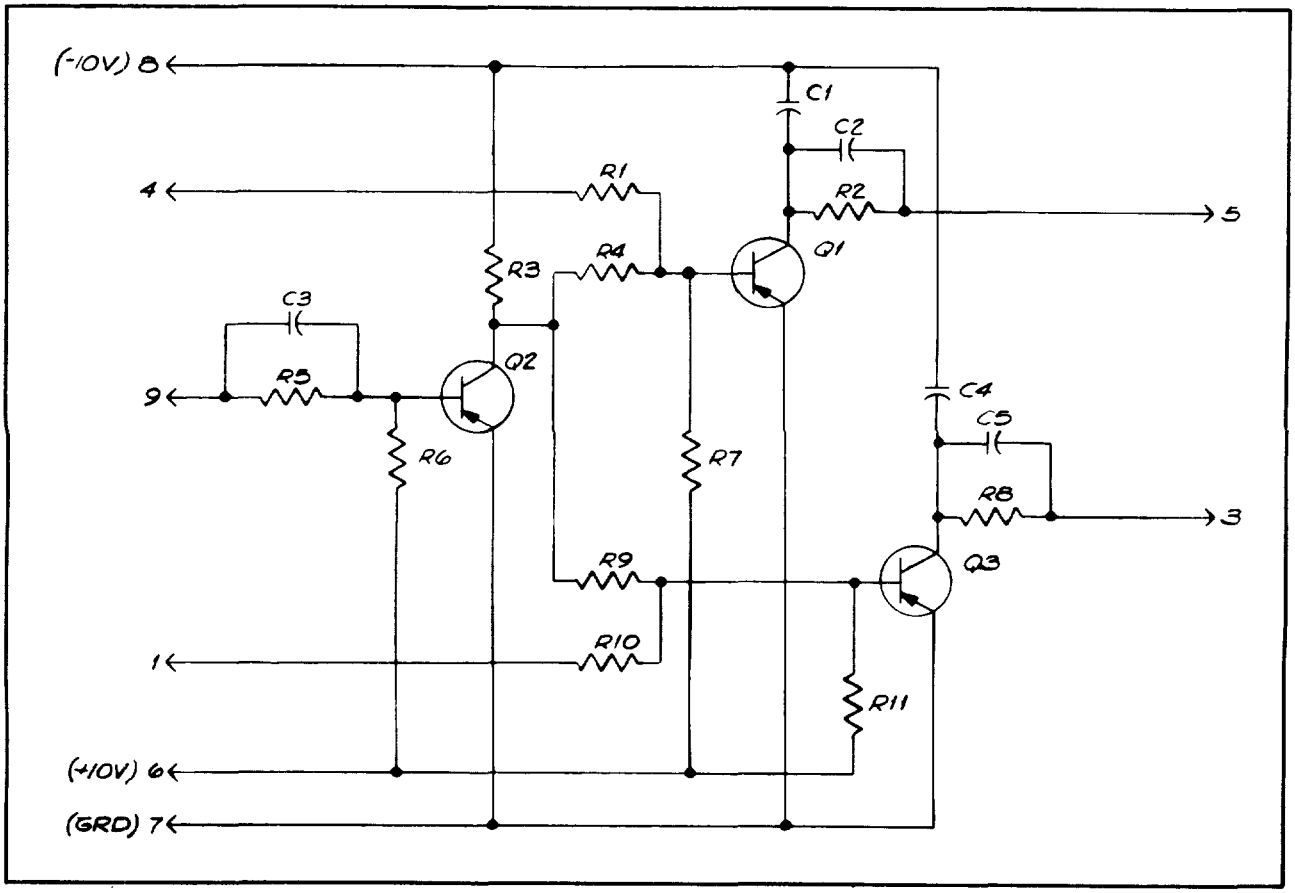


Figure 4-17. Keyer Switch

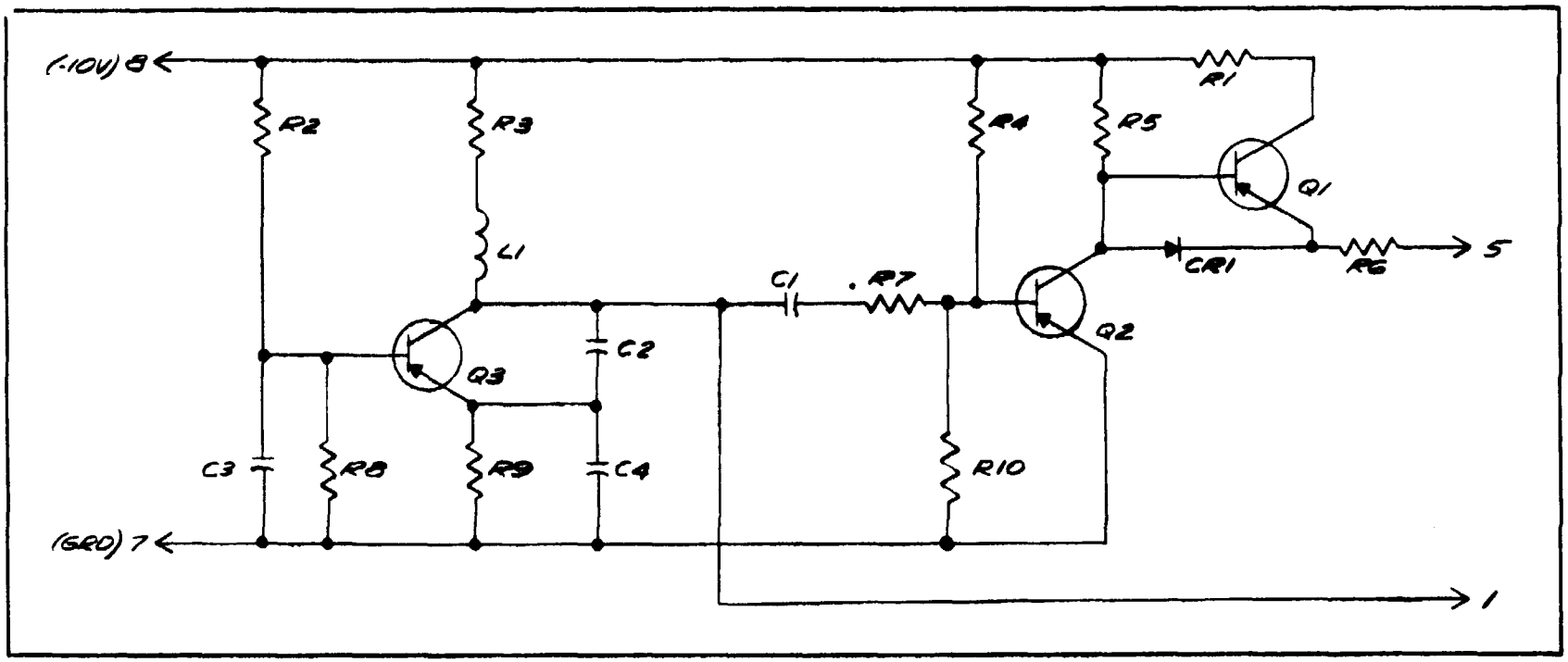


Figure 4-18. Keyer Oscillator

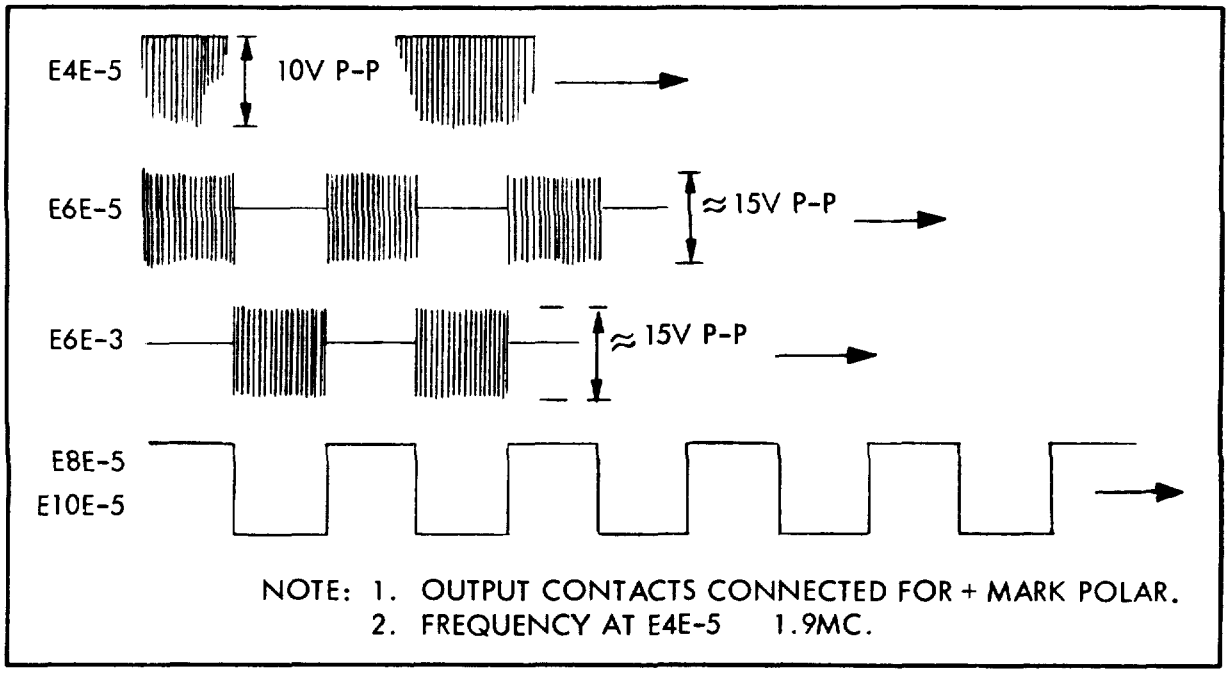


Figure 4-19. Output Keyer Timing Diagram

4-35. OUTPUT KEYER

One input of the keyer switch (see figure 4-17) is connected to 1.9 megacycles, supplied by the keyer oscillator (see figure 4-18). The other inputs of the keyer switch are connected to the mark and space outputs of the distortion control circuits. The 1.9 mcs is gated to the mark keyer by a mark input to the keyer switch and to the space keyer by a space input to the keyer switch. The 1.9 mcs signal causes a closure between the tongue output contact and the mark or space output contact.

4-36. STANDARD INTERFACE OUTPUT

The standard interface output is a signal corresponding to the keyer output, with +6 volts representing a mark condition and -6 volts representing a space condition. These potentials are supplied from an external source and are connected to the mark and space contacts of the keyer.

4-37. FORMAT CARD PROGRAMMING

Programming the Baudot Format card requires only that jumper wires be connected between appropriate points. The schematic diagram, Figure 4-14, shows a Baudot card programmed for the "quick brown fox" message. Table 4-2 shows the standard message as normally factory-programmed.

The row of 128 diodes across the card, corresponding to characters in the message, are numbered 1 through 128 and every tenth diode is identified by number on the back of the card, i.e., 1, 10, 20, etc. A jumper from one of the 128 diodes to one of the groups of lands at the top of the

card will connect that numbered character in the message to the letter or function which is printed adjacent to the group of lands.

At the end of the programmed message, the next following diode is jumpered to the "ADVANCE" line. This causes the format sequence counter to be jumped to a count of 124, preventing the Transmitter from sending a long series of letter shifts where the total possible number of characters are not used.

To add to the programmed message, the following sequence of operations is required.

Disconnect the jumper to the "ADVANCE" line. Connect that same diode to the "CR" group to program a carriage return. The next diode in sequence then should be connected to "LF, " for a line feed. Since the last character in the message was an upper case character, the next operation should be a letter shift. Letter shift is accomplished by leaving a character open, so the next diode should be left unconnected.

Now the desired letters may be programmed in direct order by jumpering. The group of lands following the letter "Z, " labeled B, are ,for a blank. Following the blank in order are FIG. (figure shift), SP (space), CR (carriage return) and LF (line feed). Again, a letter shift (LTR) is programmed by leaving a character open.

After the last desired character is programmed, the next diode in order should be connected to the "ADVANCE" line.

TABLE 4-2

STANDARD BAUDOT MESSAGE

Sequence Number	Character Programmed	Sequence Number	Character Programmed
1	T	36	SP
2	H	37	L
3	E	38	A
4	SP	39	Z
5	Q	40	Y
6	U	41	SP
7	I	42	D
8	C	43	O
9	K	44	G
10	SP	45	FIG
11	B	46	J (')
12	R	47	OPEN (LTR)
13	0	48	S
14	W	49	SP
15	N	50	B
16	SP	51	A
17	F	52	C
18	O	53	K
19	X	54	SP
20	SP	55	FIG
21	J	56	Q (1)
22	U	57	W (2)
23	M	58	E (3)
24	P	59	R (4)
25	E	60	T (5)
26	D	61	Y (6)
27	SP	62	U (7)
28	O	63	I (8)
29	V	64	O (9)
30	E	65	P (0)
31	R	66	ADVANCE
32	SP	↓	OPEN
33	T	126	CR
34	H	127	CR
35	E	128	LF

SECTION V

CHECKOUT PROCEDURES

5-1. GENERAL

The following procedures provide a method for checking the operational performance of the DAS-10 system.

The functions of the equipment are checked as relative operations in the complete system.

All installation connections should be made as shown in figure 5-1; the Data Analyzer is connected to the Data Transmitter, and the A-Scan is connected to the Data Analyzer for its signals.

The Transmitter is checked first, the Analyzer second, and the A-scan third.

After the power inputs to the DAS-10 system have been connected, the POWER switch on the Data Analyzer is switched ON, the POWER switch on the A-scan is switched ON, and the POWER switch on the Data Transmitter is switched ON.

5-2. SPECIFIC CHECKOUT PROCEDURES

5-3. DATA TRANSMITTER CHECKOUT (Model 7413 and 7413A)

Step 1 Set BIAS DISTORTION switch to ZERO position.

Step 2 Set BAUD RATE switch to 45.5.

Step 3 Set CODE LEVEL switch to START/STOP 5.

Step 4 Set RELEASE INFO switch to FREE RUN mode.

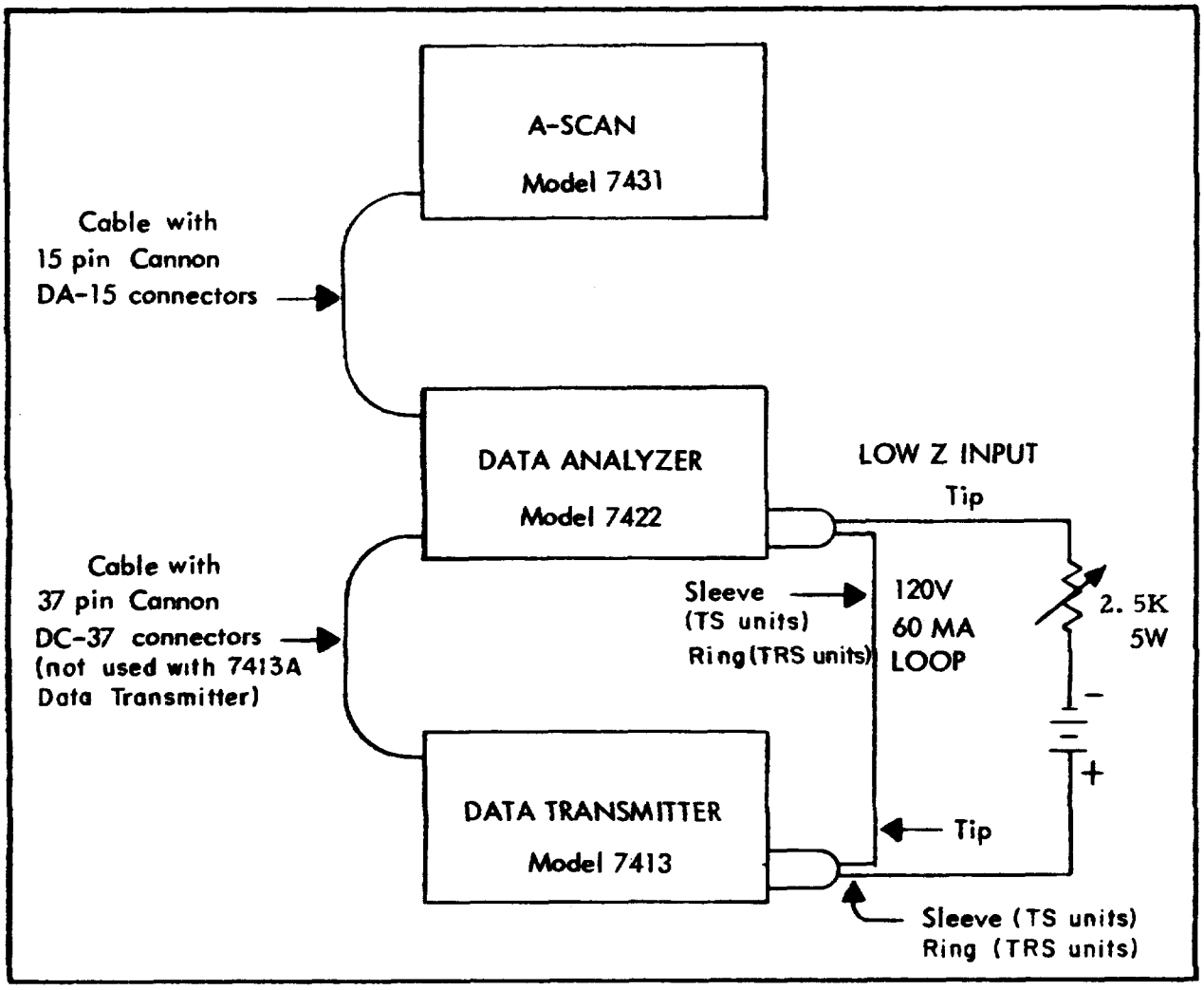


Figure 5-1. Cabling Interface

Note

Set Data Analyzer switches and controls as called out in steps 5 through 14

Step 5 Set Data Analyzer BAUD RATE switch to 45.50.

Step 6 Set UNIT INTERVALS switch to position 7.

Step 7 Set START/STOP SYNCHRONOUS toggle-switch on Analyze to START/STOP.

Step 8 Set CLOCK SELECT switch to INT XTAL.

Step 9 Set DISTORTION SELECT switch on Analyzer to AVG.

Step 10 Set AUTO-MAN RESET switch on Analyzer to center position

Step 11 Set INPUT SELECT LOW Z switch on Analyzer to 60 MA NEUTRAL.

Step 12 Set Analyzer POLARITY switch to MINUS.

Step 13 Set Analyzer FILTER switch to OUT.

Step 14 Set Analyzer MARK-SPACE SPACE-MARK toggle-switch to SPACE/MARK position.

Note

Set A-Scan switches and controls as called out in steps 15 through 18

Step 15 Set A-Scan CHARACTER BLANKING switch to OFF position

Step 16 Set A-Scan INTENSITY MARKERS toggle-switch to OFF.

Step 17 Set A-Scan SWEEP OPTIONS switch to AUTO.

Step 18 Set INTERNAL SWEEP to lowest range.

Note

The Data Transmitter is checked out in all baud ranges with ZERO distortion. The corresponding baud rates are viewed on the A-Scan each time the BAUD RATE switch on the Data Transmitter is changed to the next position. The BAUD RATE switch on the Data Analyzer must also be changed to correspond to the same baud range.

Step 19 In each baud rate position, vary the BIAS DISTORTION switch position on the Data Transmitter as follows:

Transmitter	Analyzer
1 MARKING	1 EARLY PEAK
2 SPACING	2 LATE PEAK
3 SWITCHED	3 AVG

Note

The amount of distortion shown on the A-Scan and the Data Analyzer meter should correspond with the percent of distortion fed into the equip ment. When the BIAS DISTORTION switch is in the ZERO position, the Analyzer readout should be "zero".

As distortion is selected on the Data Transmitter, the DISTORTION SELECT switch on the Data Analyzer should be to a corresponding position and the per cent of distortion should show on the Data Analyzer PERCENT DISTORTION meter.

Step 20 Check the percent distortion from 0 to 49% in the TEST MESSAGE position of the Transmitter PATTERN SELECTOR switch.

Step 21 Set Transmitter PATTERN SELECTOR switch in REVERSALS position.

Step 22 Set Transmitter RELEASE INFO switch in FREE RUN position.

Step 23 On the Transmitter BAUD RATE switch select a convenient BAUD RATE position.

Step 24 Set Transmitter CODE LEVEL switch to START/STOP 5.

Step 25 Leave switches set as above and set Transmitter BIAS DISTORTION switch to ZERO.

Note

Set up any character desired with the eight pushbutton switches of the Transmitter PATTERN SELECTOR switch and set RELEASE INFO switch to the FREE RUN mode.

Step 26 Use any convenient pattern to select the information character.

Note

The IN position of the push-button switch is a MARK, the OUT position is a SPACE.

Step 27 View the character transmitted by the Data Transmitter on the A-Scan.

Step 28 Select IDLE CHARACTER mode.

Note

The idle character is selected by slide switches internal to the Data Transmitter. (The location is shown in figure 3-2, Section III, of this manual.)

Step 29 Observe selected idle character shown on A-Scan.

Step 30 Set Transmitter RELEASE INFO switch to STEPPED position. (An external sync pulse, provided by the customer, is connected to the BNC (SYNC IN) connector on the rear of the Transmitter.)

Step 31 Observe the test message (selected on the internal PATTERN SELECTOR switches) on the A-Scan with one character released by each external sync pulse. (The SYNC POLARITY toggle-switch on the rear panel of the Data Transmitter selects the

polarity of the response to the external sync input).

Step 32 Set Transmitter RELEASE INFO switch to BIT SYNC position.

Step 33 Set Transmitter CODE LEVEL switch to 5 in SYNC position.

Step 34 Transmitter requires external synchronization signal. Set Analyzer to corresponding baud rate.

Step 35 Set SYNC START/STOP switch on Analyzer to SYNC position.

Step 36 Observe the bit presentation on the A-Scan with each external sync pulse. (The SYNC POLARITY toggle-switch on the rear panel of the Data Transmitter select the polarity of the response to the external sync input.)

Step 37 Check steady mark operation by setting Transmitter RELEASE INFO switch to STEADY MARK position.

Step 38 On the A-Scan observe a steady signal which is the normal mode of operation.

Step 39 Set TIME BASE GENERATOR CLOCK SELECT on analyzer to INTERNAL VFO and repeat steps 1 through 38.

Step 40 Set TIME BASE GENERATOR CLOCK SELECT switch EXTERNAL CLOCK and repeat steps 1 through 38 using station clock.

5-4. DATA ANALYZER CHECKOUT

Portions of the Data Analyzer have been checked out with the check-out of the Data Transmitter.

To check out the Analyzer, the A-Scan and the Data Transmitter are necessary to check the TRANSITION SELECT measurement and the additive PERCENT DISTORTION measurement.

Step 1 Set Analyzer DISTORTION SELECT switch to AVG position.

Step 2 Set Analyzer INPUT SELECT switch to 60 MA NEUT.

Step 3 Connect input signal to Analyzer LOW Z jack.

Step 4 Set Analyzer POLARITY switch to MINUS.

Step 5 Set Analyzer TRANSITION SELECT toggle-switch to SPACE-MARK.

Step 6 Set Analyzer TRANSITION SELECT rotary switch to ALL.

Step 7 Set Analyzer TIME BASE GENERATOR CLOCK SELECT switch to INT XTAL.

Step 8 Set START/STOP SYNC switch to START/STOP.

Step 9 Set Analyzer UNITS INTERVALS switch to 7.

Step 10 Set Analyzer BAUD RATE. switch to 45.5.

Step 11 Set Transmitter BAUD RATE switch to 45.5.

Step 12 Set Transmitter CODE LEVEL switch to START/STOP 5.

Step 13 Set Transmitter PATTERN SELECTOR switch to TEST MESSAGE.

Step 14 Set Transmitter RELEASE INFO switch to FREE RUN.

Step 15 Check pattern transmitted by the Transmitter on the CRT of A-Scan and on the meter of the Analyzer.

Step 16 Check the capability of the Analyzer to measure percent distortion in 1% increments by setting Transmitter BIAS DISTORTION switch to MARKING position and

Step 17 Vary Transmitter PERCENT DISTORTION thumbwheel switches from 1% to 49% in 1% steps.

Note

The Analyzer AUTO MAN RESET switch in AUTO position will update the Analyzer every 4-1/2 seconds.

Step 18 Set Analyzer DISTORTION SELECT switch to TOTAL PEAK position and read total distortion number (on meter) fed into the Analyzer by the Transmitter.

Step 19 Set Transmitter BIAS DISTORTION to SPACING position.

Step 20 Vary the PERCENT DISTORTION thumbwheel switches on the Transmitter from 1% to 49% and read the results on the Analyzer.

Step 21 Set the DISTORTION SELECT switch on the Analyzer to EARLY PEAK/LATE PEAK positions to correspond with the MARKING and SPACING distortion supplied by the Transmitter.

Step 22 On the Transmitter select a BIAS DISTORTION switch

position and select total peak on DISTORTION SELECT switch on the Analyzer, and read corresponding distortion on Analyzer meter.

Note

The above tests can be re-run by selecting different baud rates on both the Transmitter and Analyzer.

Step 23 Checkout the 20 MA NEUT position on the Analyzer INPUT SELECT LOW Z switch by repeating steps 1 through 20 of paragraph 5-4.

Step 24 After adjustment of the 20 MA supply into the Analyzer, re-run steps 1 through 20 of paragraph 5-4 for the Analyzer 60 MA switch position.

Step 25 Insert signal in the HIGH Z jack of the Analyzer and repeat the above 20 steps for the INPUT SELECT switch positions of HIGH V MED V and LOW V.

Note

The UNITS INTERVALS in the Analyzer are checked at 7, 8, 9, 10 and 11 bit positions on the Transmitter CODE LEVEL switch to the START/STOP 8 position to correspond with the 11 position on the UNITS INTERVALS switch on the Analyzer. Stop increments of 2.0 must be supplied by the Transmitter. This requires Transmitter slide-switch positioning. (See figure 3-2, Section III of this manual)

Step 26 Repeat steps 1 through 25 with Analyzer CLOCK SELECT switch in INT VFO position to provide the time base.

Step 27 Repeat steps 1 through 26 with Analyzer TIME BASE GENERATOR SELECT switch in EXT CLOCK position using external station clock.

5-5. A-SCAN CHECKOUT

The A-Scan is intended for use as a slave oscilloscope to display the signal received by the Analyzer. The A-Scan cannot be used alone as it receives both power and control signals from the Analyzer.

The cathode-ray tube (CRT) is a flat-face five-inch tube with a long-persistence screen. The face of the tube has a graduated scale corresponding to 5 and 8-unit codes, with horizontal and vertical graduations to permit using the A-Scan as a current or voltage-indicating device. It has an accuracy of ± 5%.

Step 1 Check intensity modulation. Observe that trace is intensified to indicate the sampling points on the input wave form used by the Analyzer for distortion measurements. (When a transition is selected by the Analyzer the associated segment will be intensified on the A-Scan screen. The sampling point on the selected transition is shown by an intensification - return to normal - and back to intensification.)

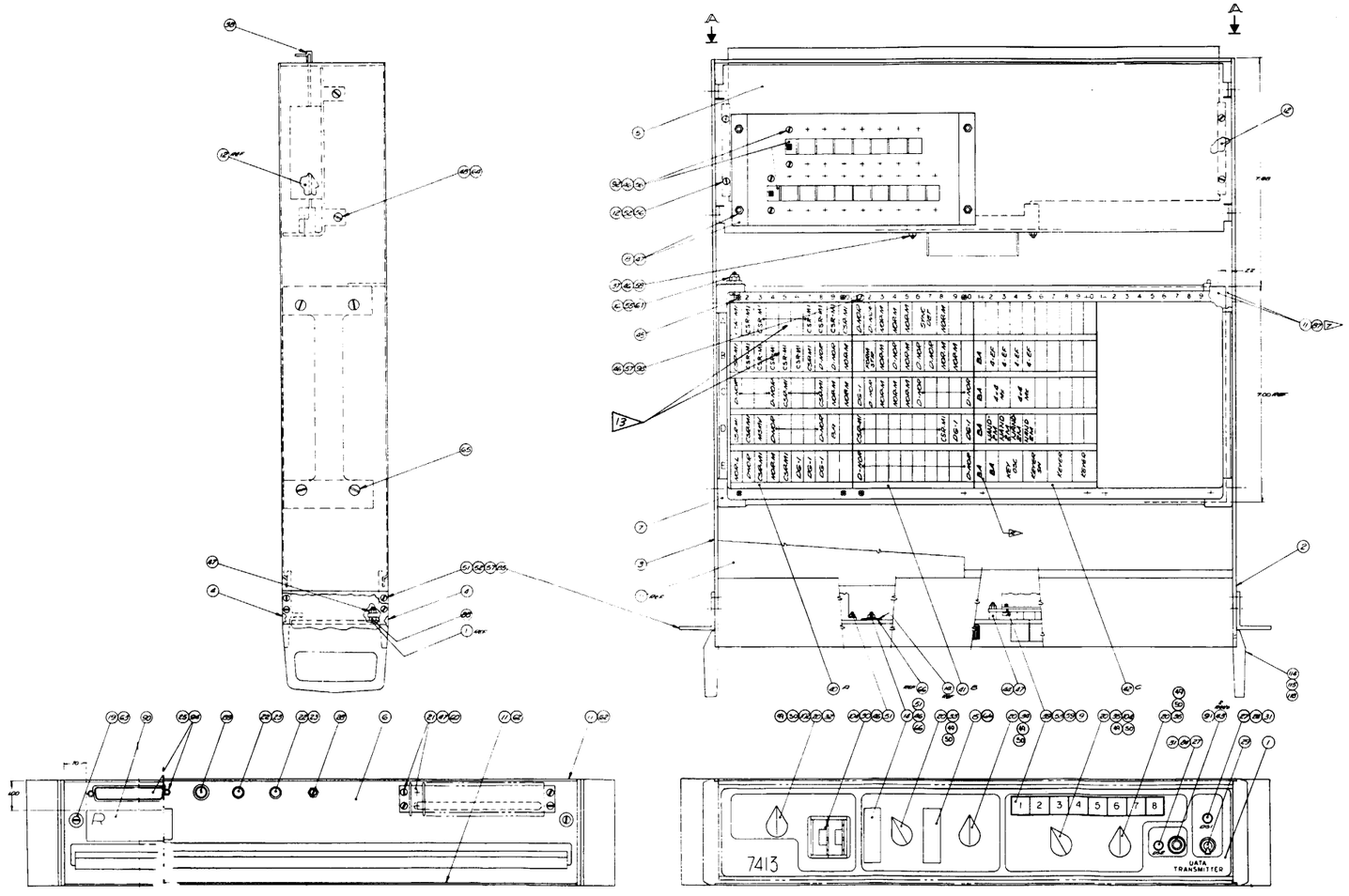
Step 2 Check character blanking. (The direct-coupled gate signal

is supplied to the CRT to blank the trace during retrace and waiting periods). The gate signal is supplied to the CRT to blank the display in a variable pattern which is selectable by front-panel controls. A single sweep may be followed by a blank display for two, three, four, five or six character intervals or for an indefinite interval. The sweep must be reset each time for single display.

Step 3 Check internal sweep time periods. (The sweep time period can be varied from 250 microseconds to 300 milliseconds). The sweep times accommodate all baud rates from 25 bauds to 9600 bauds. (The sweep linearity is ± 2%.)

Step 4 Check synchronization. In the AUTO SWEEP OPTION (START/STOP only) the Analyzer starts the saw at the leading-edge of the START pulse and unblanks the CRT. In the TRIGGERED SWEEP OPTION the Analyzer supplies a synchronization pulse at the beginning segment of the selected character and permits viewing of the transition selected for analysis. In FREE SWEEP OPTION the AUTO sweep is not synchronized.

Step 5 Check horizontal input. (A horizontal saw is generated by the Analyzer for STOP/START signal display.)



NOTES

12 MODULES IN LOCATION C1B-C1E AND C2E ARE USED ON G2 ASSEMBLY ONLY.

13 MODULE CSR-M4 TO BE USED IN PLACE OF CSR-M1 AT LOCATIONS A4B-A7B AND MODULE CSR-M3 TO BE USED IN PLACE OF CSR-M1 AT LOCATIONS A3A-A7A ON G3 ASSEMBLY.

Figure 5-2. Data Transmitter Assembly.

SECTION VI

GENERALIZED SYSTEM TROUBLESHOOTING

PROCEDURES

6-1. GENERAL

A clear understanding of the principles of operation of this equipment is necessary before successful troubleshooting can be accomplished. It is recommended that the appropriate PRINCIPLES OF OPERATION section elsewhere in this manual be used as a basis for logical analysis and solution of equipment failures. All test points (pin 10) of all modules are connected to pin 11 of all modules and are available by inserting the oscilloscope test probe into the test point in front of each module on the "Mother Board." This is true for both Transmitter and Analyzer.

CAUTION

Do not use wire-wrap terminals on the back of boards for test points for troubleshooting. It is noted that arbitrary replacement of an inoperative module may result in further failures if the cause of the initial failure is not clearly established. For example, in the Model 7413 Transmitter (fig. 4-2), a failure in Emitter-Follower module, C2B to C5B, may result in the failure of a Counter Shift Register module A4B to A7B. Replacement of the faulty CSR module before removal of the cause of failure can only result in another CSR failure.

The following example will serve as an illustration for a generalized troubleshooting procedure.

6-2. SYMPTOMS

1. Clock Failure Light ON.
2. Audible Alarm SOUNDING.
3. Appears to Work Above 150 Bauds, not Below.

6-3. PROCEDURE USED TO LOCALIZE TROUBLE

Step 1. Push ALARM SILENCE button. (CLOCK FAILURE light remains lighted.)

Step 2. Examine B1E10, B2E10, B3E10, B4E10, B5E10, B6B10, B7E10, B8B10, B9E10, and B10E10 consecutively for waveforms shown in figure 4-3 Part B of this manual to determine at what point the signal was lost. (In this ex ample the signal does not appear at B10E10 because of a defective CSR-M1 module.)

6-4. CORRECTIVE ACTION

Step 3. Replace defective CSR-M1 module in location B10E and examine output for proper waveshape. CLOCK FAILURE light should go OUT.

Note

Similar troubleshooting techniques using logic diagrams and waveforms are used for other problems.

SECTION VII

DATA TRANSMITTER 7413 A

7-1. INTRODUCTION

The Model 7413A is a modified version of the standard 7413 Data Transmitter.

The addition of an internal power supply and a self contained time base generator (clock and clock divider) allows the 7413A to function independently of the DAS-10 Analyzer.

The following is a brief description of the circuits added to the Model 7413 to convert to a Model 7413A. Refer to 7413A Logic Diagram, figure 7-1.

7-2. GENERAL: CLOCK DIVIDER

The clock divider is a 10-stage binary counter using CSR-MI modules connected for counter applications. When operated as a straight divider binary chain, baud rates 37.5, 75, 150, 300, 600, 1200, 2400, 4800 and 9600 are available. Other baud rates, which do not bear binary relationship to 75 bauds, are accomplished by programmed presetting of the clock-divider chain. Out put from the clock divider is a frequency equal to 100 times the selected baud rate.

7-3. DETAILED PRINCIPLES OF OPERATION

7-4. CLOCK DIVIDER (See Logic Diagram, Figure 7-1).

A crystal oscillator module (C1A-C2A) generates the Basic timing for the 7413A Transmitter. The frequency of operation of this oscillator is 3.84

mHz.

The input stage of the clock divider (C3A) is a CSR-M module connected as a buffer inverter. This inverter supplies a 3.84- mc clock signal to the trigger input of the first flip-flop in the clock -divider chain. Baud rates of 37.5, 75, 150, 300, 600, 1200, 2400, 4,800, and 9600 are tapped directly by the BAUD RATE, switch shown in the logic diagram. The programmed pre-setting system, used in this clock-divider chain, permits generation of over 1000 additional non-integer baud rates. Baud rates that are not binary functions of 3.84- mc are provided by programmed presetting of the clock-divider chain.

7-5. PROGRAMMING COUNTER CHAIN FOR BAUD RATES

Assuming the first flip-flop (C4A) has a binary weight of 2^0, then the following stages appear as 2^1 through 2^9. A binary weight of 2 on the first flip-flop permits the use of a 3.84-mc timing source. To obtain a frequency from the clock divider of 5560-cycles-per-second (100 x 55.6 baud) a flip-flop output must be selected which has a slower counting rate, and numbers are then injected into, the counter to increase the speed. For 5560 cycles/sec the output is obtained from the 2^9 stage (normally 3750 cycles/sec).

If the timing source (3.84- mc) is divided by 5560 and rounded off, the nearest whole number will be 691.

The full count of the clock divider chain is 1024.

For example:

1024 - 691 = 133

333 256 + 64 + 8 + 4 + 1

Therefore, for an output of 5560 cycles/sec, the 256, 64, 8, 4 and 1 flip-flops must be set at the beginning of each cycle.

This presetting is (lone via the BAUD RATE switch and patch jumpers located in module locations C9D, C10D, C9C, C10C, C9B, C10B, C9A and C10A. A CSR-Ml module (C7D) produces a pulse of approximately 140 nano seconds to accomplish this presetting. The 1/2 Dual-NOR module (in location C6D), wired as a power driver, provides the pulse amplitude required to preset the number of flip-flops involved.

7-6. POWER SUPPLY

The 114534-1 Power Supply provides the necessary plus and minus 10 volts for Radiation Digital Logic Modules and other additional circuits. The power supply is designed specifically to mount in a module frame. It mounts in the same space normally required for one contact board. The over-all height of the mounted power supply is less than 3.5 inches. The characteristics of this power supply are listed below:

INPUT: 117V rms ± 10% 47 to 400 cycles.

OUTPUT: - 10V ± 1 % at 2.2 amp maximum 110V ± 1% at 0.2 amp maximum. All outputs to be DC isolated from chassis.

RIPPLE: Less than 10 mV rms, both channels

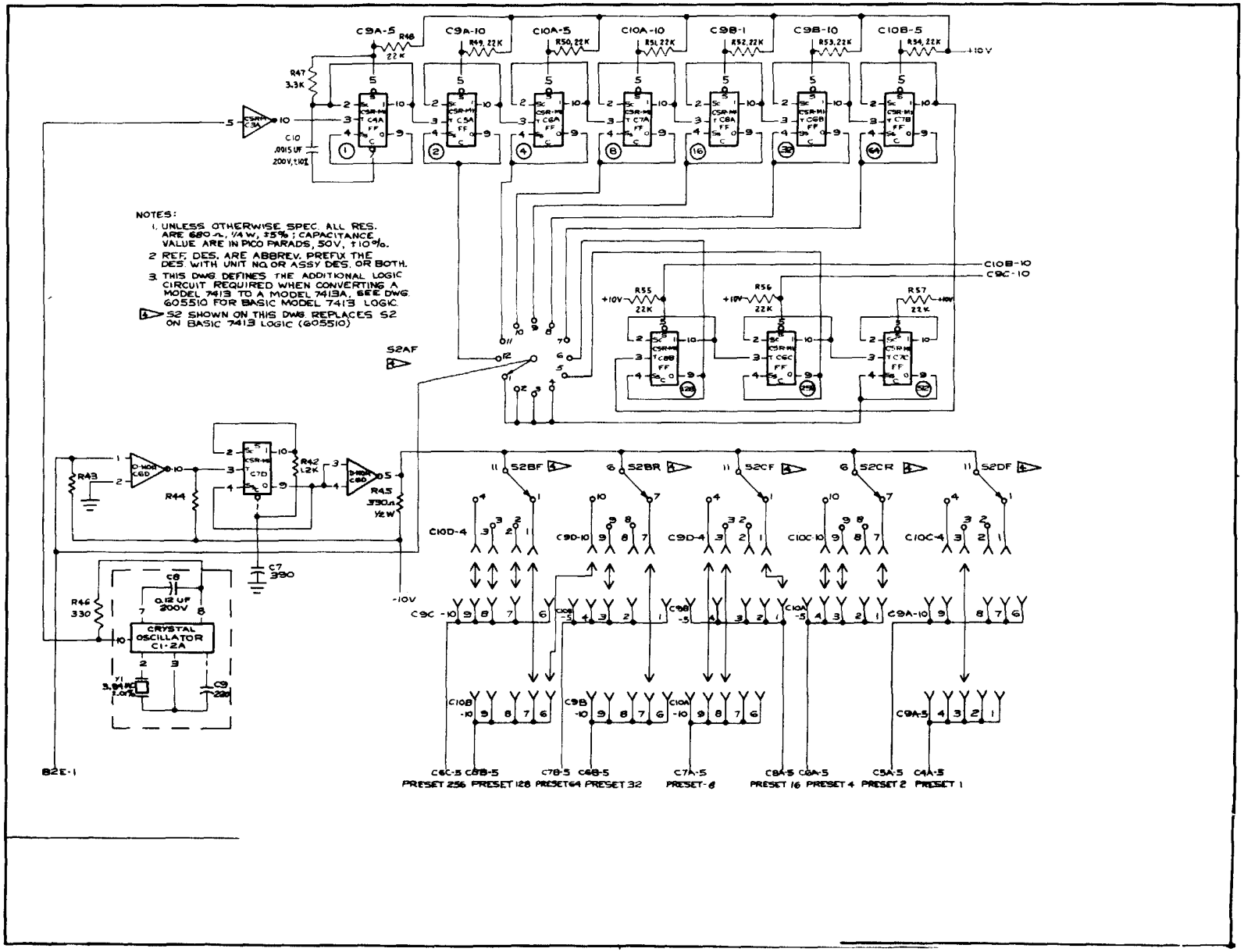


Figure 7-1. Logic Diagram, 7413A Clock Divider

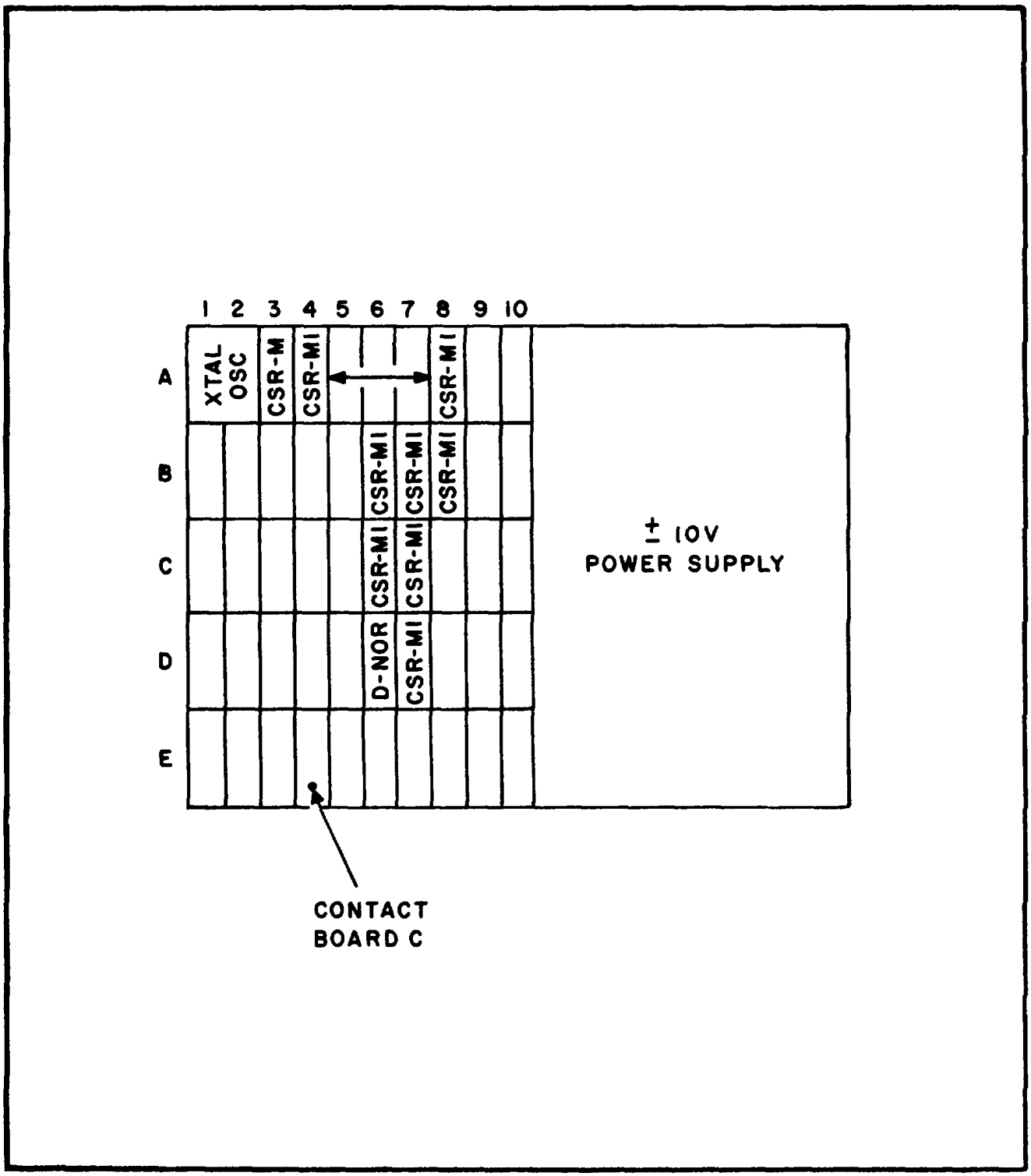


Figure 7-2. Module Location Diagram.

7-7. Power Supply Circuit Functioning
(fig. 7-3)

Both sections of the power supply operate in an identical manner. Each output consists of an unregulated full-wave dc supply using a capacitive filter, a series regulator consisting of transistors Q101 or Q102 and Q103, common emitter driver Q3, and error amplifier Q1. A portion of the output voltage is compared with the reference voltage developed across diode CR4 at the base emitter junction of transistor Q1. The output of Q1 controls transistor Q3 and, therefore, transistors Q101 or Q102 and Q103, thus regulating the output voltage. The output current of the power supply is sampled by the voltage drop developed across resistor R1, and the output voltage is sampled by the voltage drop developed across resistor R4. The sum of these two voltages is compared to the voltage drops across diode CR3, resistor R5, and the base emitter voltage of transistor Q2. Current drain in excess of the value determined by the setting of resistor R4 will drive transistor Q2 toward saturation. Transistor Q1 will have no affect (bypassed) at this time, and transistor Q3 will be driven toward saturation. Series regulators Q102 and Q103 or Q101 will act to decrease the output current at this time.

7-8. Power Supply Adjustments

f the power supply output voltage changes from its rated value due to aging of components, adjust resistor R14 to obtain the correct output voltage (10 vdc). If the power supply regulation is defective, the output voltage will vary (above or below tolerance) at load values below the maximum rating. To reset the series regulators, connect an ammeter in series with the load and adjust potentiometer R4 until the output just begins to drop from its regulated point with the load current 5% in excess of the rated full load value.

7-9. Power Supply Troubleshooting

Most of the power supply troubles will be caused by faulty transistors. One of the most common failures will be collector-to-emitter shorts in series regulators Q101, Q102, and Q103. Indications of this failure will be a rise in the output voltage above the normal regulated value, loss of regulation, and increased ripple in the output circuit. An open circuit in transistor Q1 or Q3 will produce a high unregulated output voltage. Normal input voltage across filter capacitor C101 or C103 and no output voltage can be caused by open series regulator Q101, Q102, or Q103. Shorted transistor Q1, Q2, and Q3 can also cause this condition. If zener diode CR4 is shorted, low output voltage will result. If fuse F101 fails when input power is applied, check diodes CR1 and CR2 and filter capacitors C101 and C103 for shorted conditions.

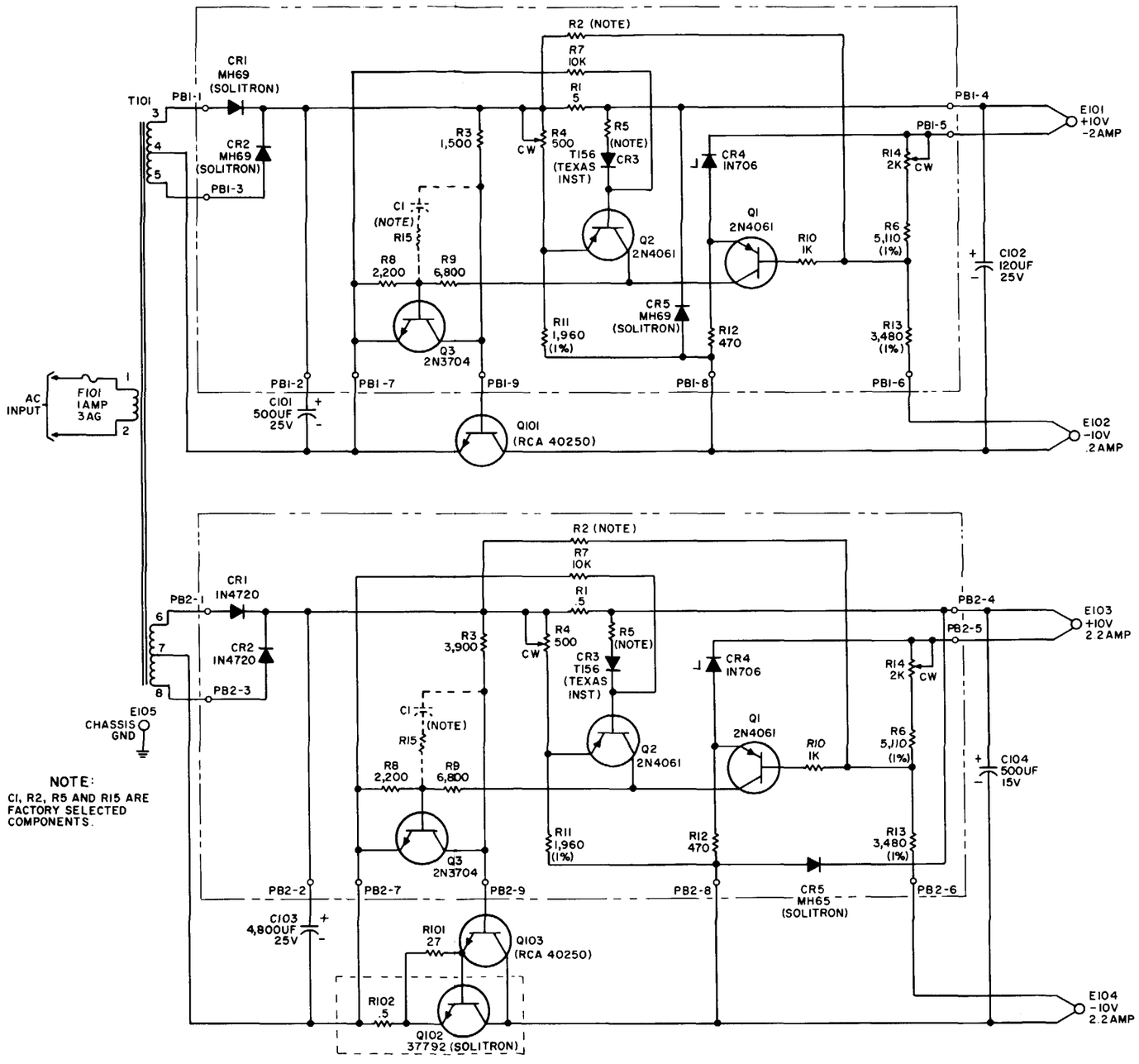


Figure 7-3. Power Supply 114534-1 (Model 6145), schematic diagram.

SECTION VIII

SPECIAL MODULES

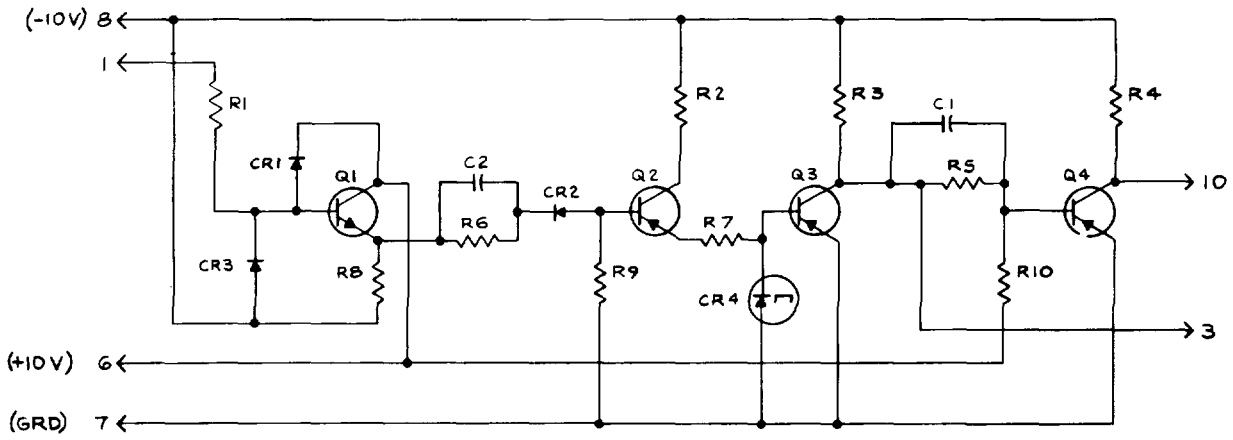


Figure 8-1. Sync Input Detector (Module 514111)

The Sync Detector module is a threshold detector circuit which accepts a polar signal of 2 to 20 volts peak-to-peak and generates a 0 to -10 volt pulse, together with its complement.

Q1 is an emitter follower with its base clamped by diodes CR1 and CR3, which limit the voltage excursion of the base to + or -10 volts. The output of Q1 controls Q2, which serves as a current source for tunnel diode CR4 and the base of Q3. As current through the tunnel diode changes level, the diode switches across its negative resistance region causing Q3 to be rapidly switched on or off. Q4 is an inverter to provide the complement of the output from Q3.

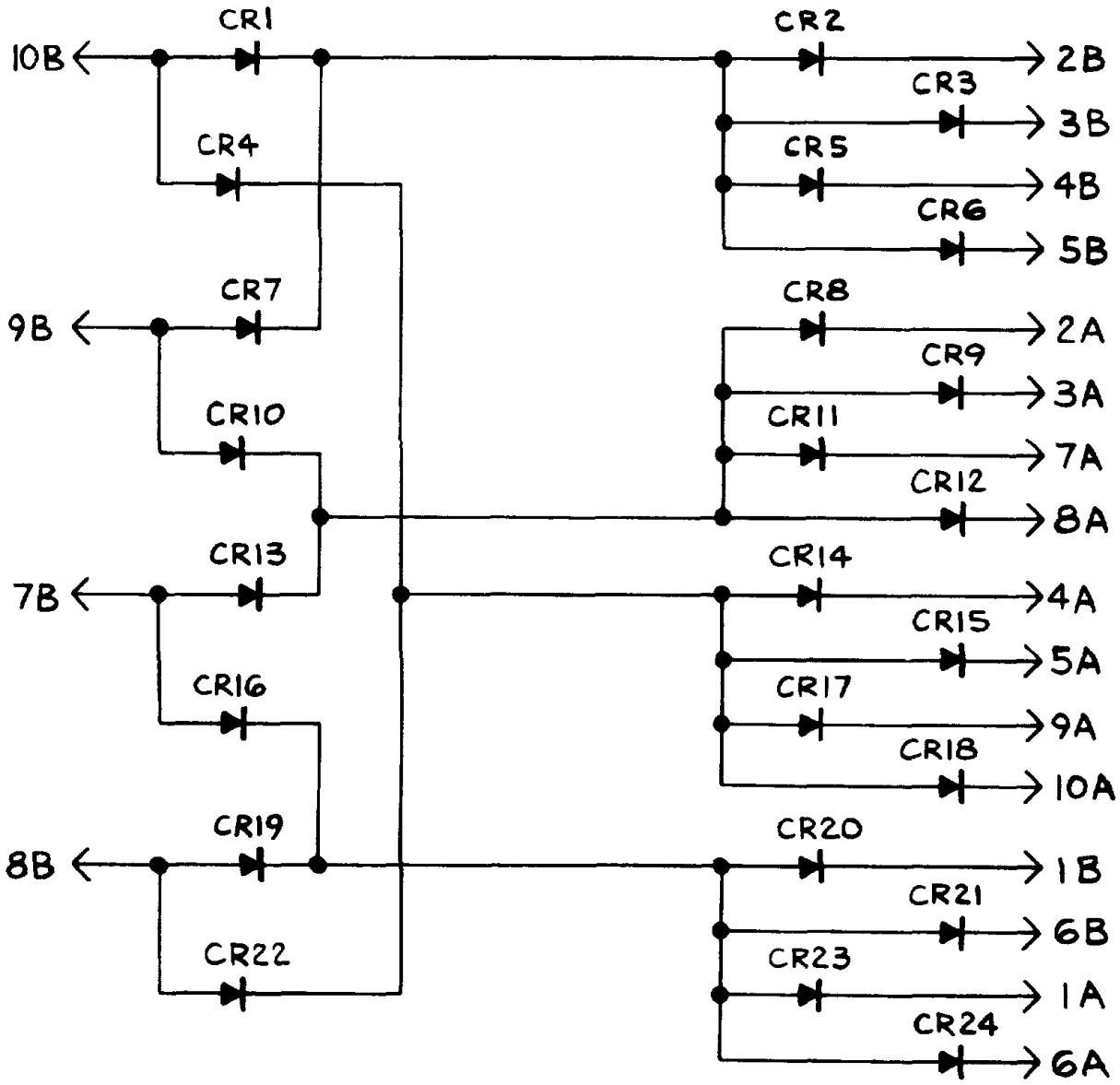


Figure 8-2. 4 x 4 Mx (Module 514113)

The 4 x 4 Mx module is a diode matrix circuit. Two of these modules are inter-connected so as to decode the number content of the second section of the format sequence counter, from 0 through 15.

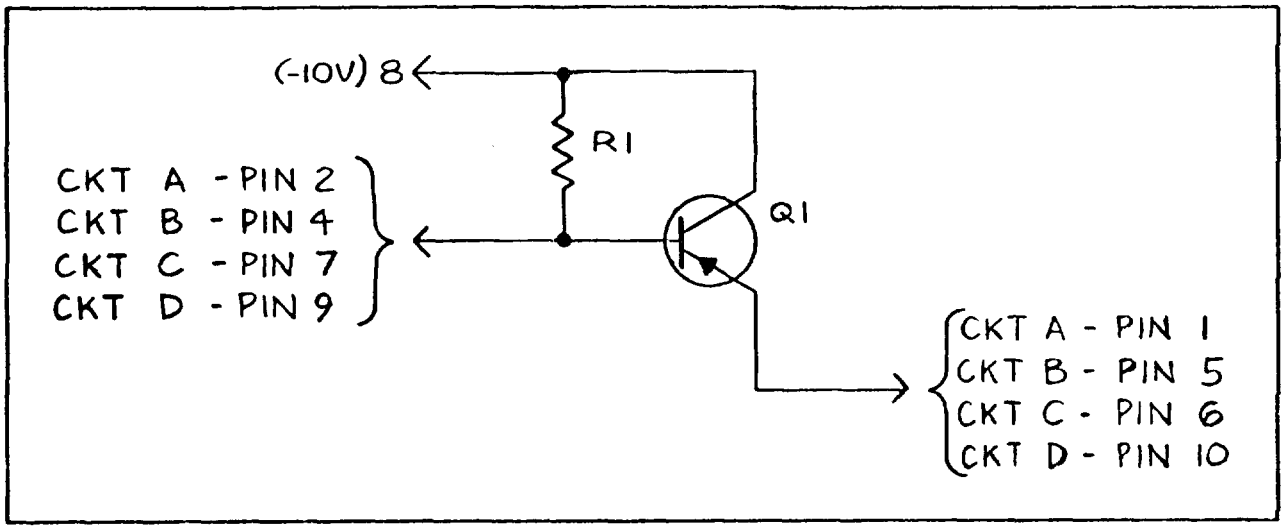


Figure 8-3. 4-EF (Module 514116)

This module consists of four identical emitter follower circuits. The emitter follower output signal is identical to the input, and has a high current-drive capability for the purpose of supplying eight of the resistor-diode gates on the Format Card.

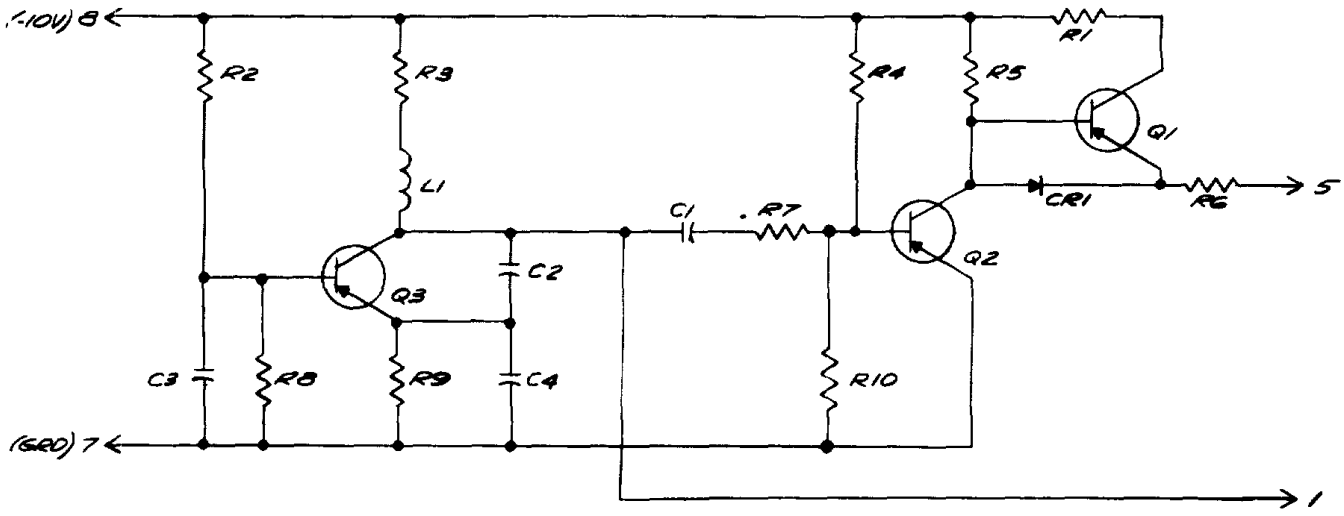


Figure 8-4. Keyer Oscillator (Module 514115)

Transistor Q3 and its associated components comprise an oscillator which is tuned to approximately 1.9 mc by an external tuned circuit connected between pins 1 and 7. Q2 amplifies the oscillator output to logic level and Q1 is an emitter follower which provides a low impedance output and prevents Q2 from being loaded down.

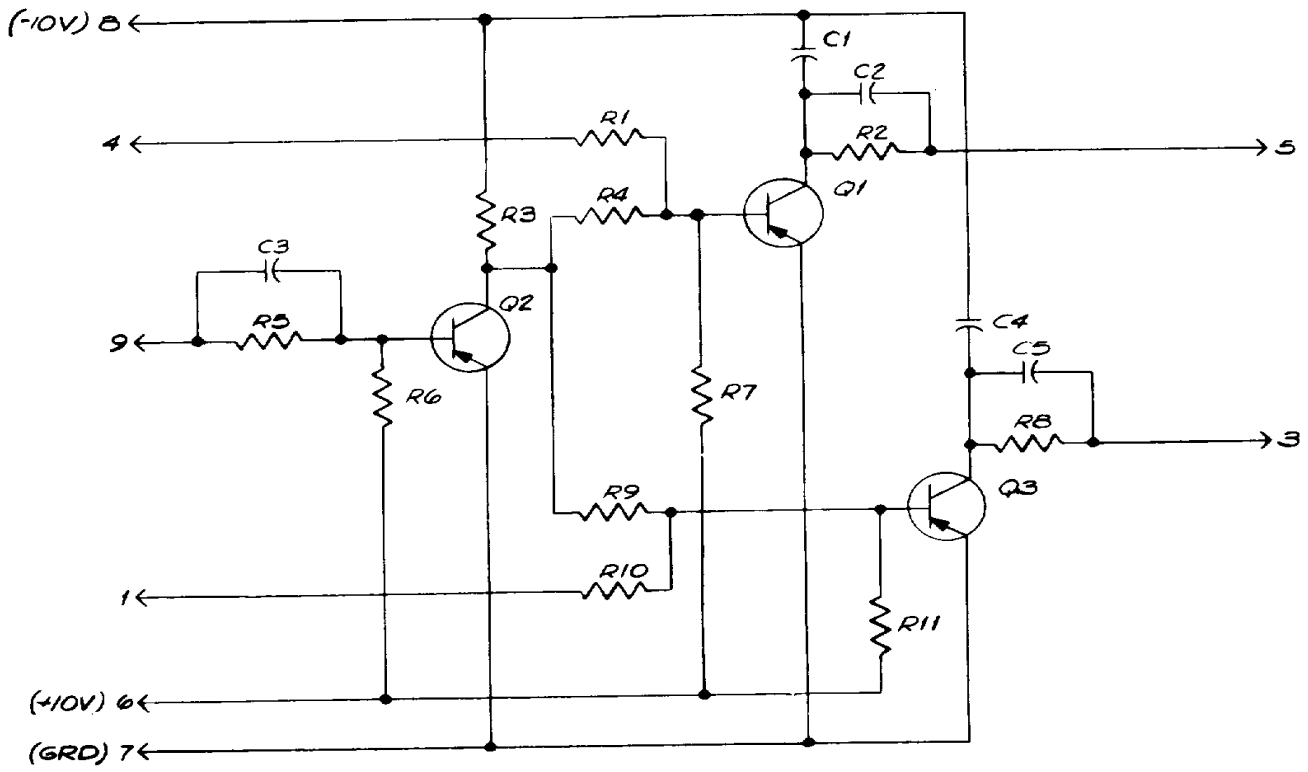


Figure 8-5. Keyer Switch (Module 514112)

The Keyer Switch module is composed of a buffer circuit for the 1.9 mc drive signal and two NOR circuits with tuned outputs.

The 1.9 mc is applied to the inputs of both NOR circuits by the buffer. The other input of each NOR is switched to a negative logic level to inhibit the 1.9 mc or to a 0 level to allow the 1.9 mc to appear at the output.

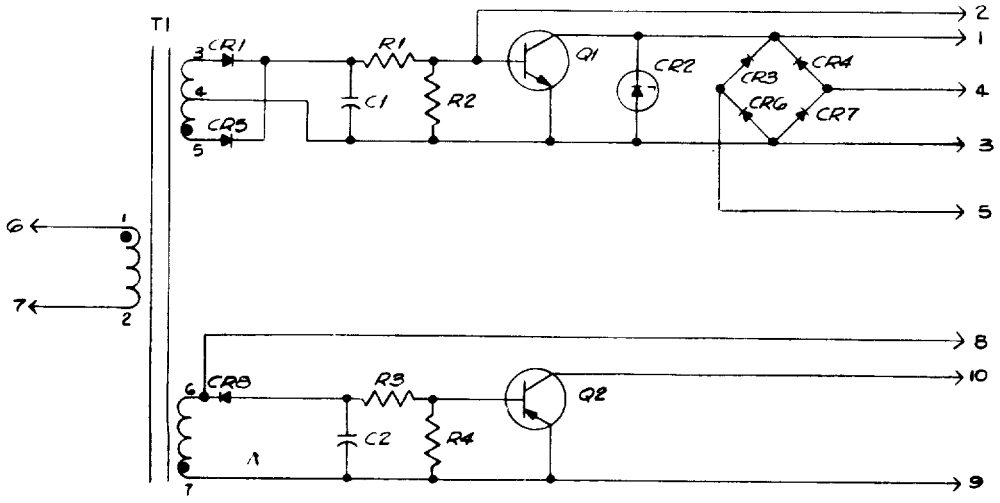


Figure 8-6. Keyer (Module 514114)

The Keyer module is designed to provide high-level keying capability while maintaining dc isolation from the internal logic circuitry of the Transmitter.

When a 1.9 mc drive signal is applied to the primary of input transformer T1, it is rectified and applied to the base of power transistor Q1. The transistor is driven into saturation, causing pins 4 and 5 to look like a short circuit, or "closed contacts, " through the diode bridge. Use of a bridge circuit allows the output to switch either polarity of current. Zener diode CRZ provides over-voltage protection for Q1.

At the same time Q1 is saturated, Q2 is also driven into saturation. The emitter and collector of Q2 are connected between the base and emitter of Q1l in the opposite Keyer module, to speed up turn-off of that Keyer when the data changes state.

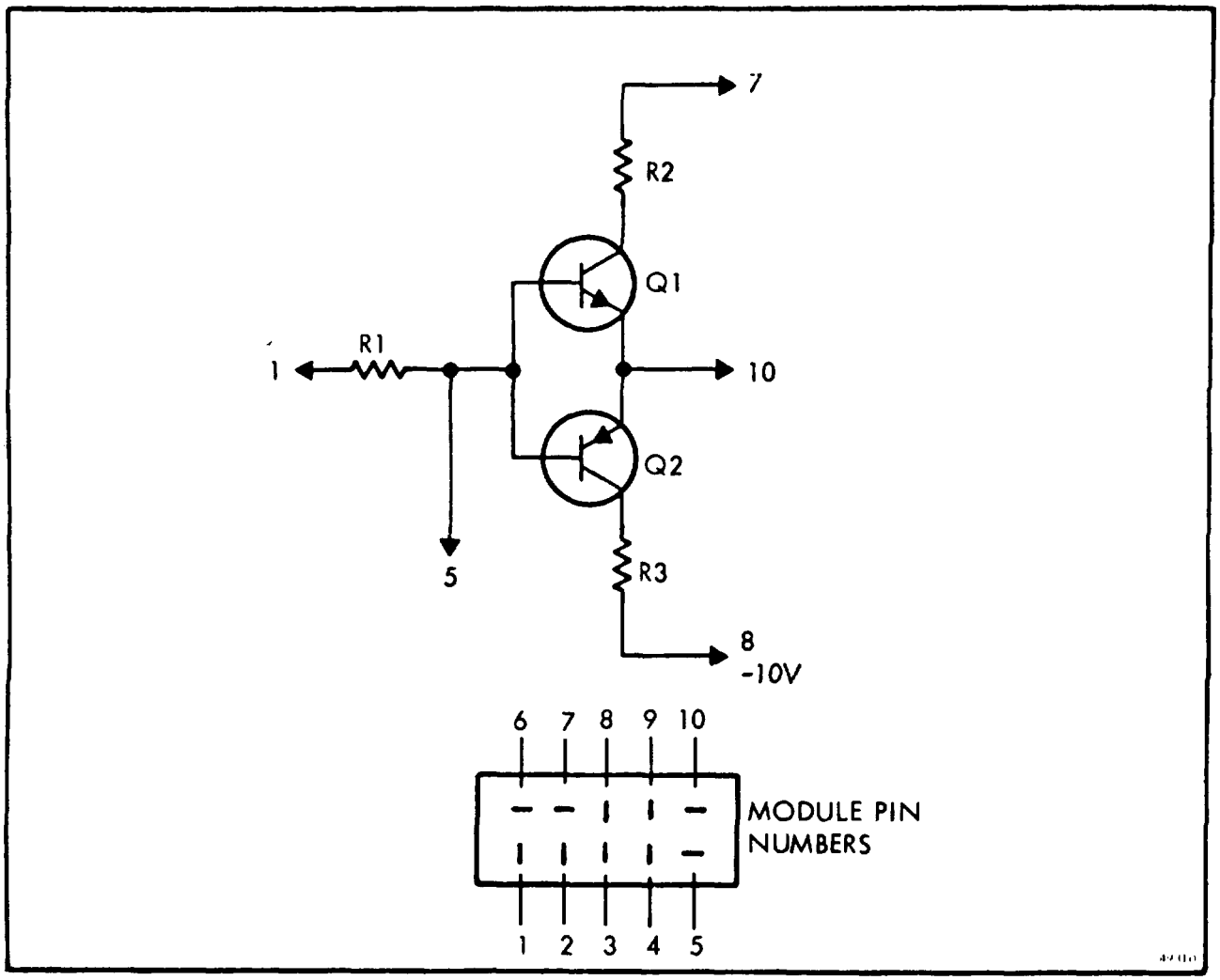
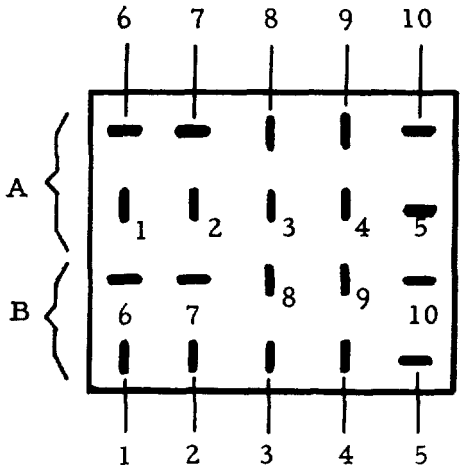


Figure 8-7. Buffer Amplifier (Module 506065G2)

The circuit is a complementary emitter-follower and is used, when needed, to provide larger fan-out capability.

The input resistor (R1) isolates the driving circuit from any capactive loading on the output.

The Buffer Amplifier adds negligible delay to low or medium-speed input waveforms.



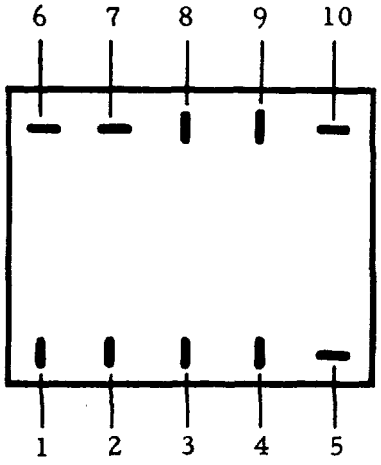


Figure 8-8. Base Diagram, Double-Size Modules

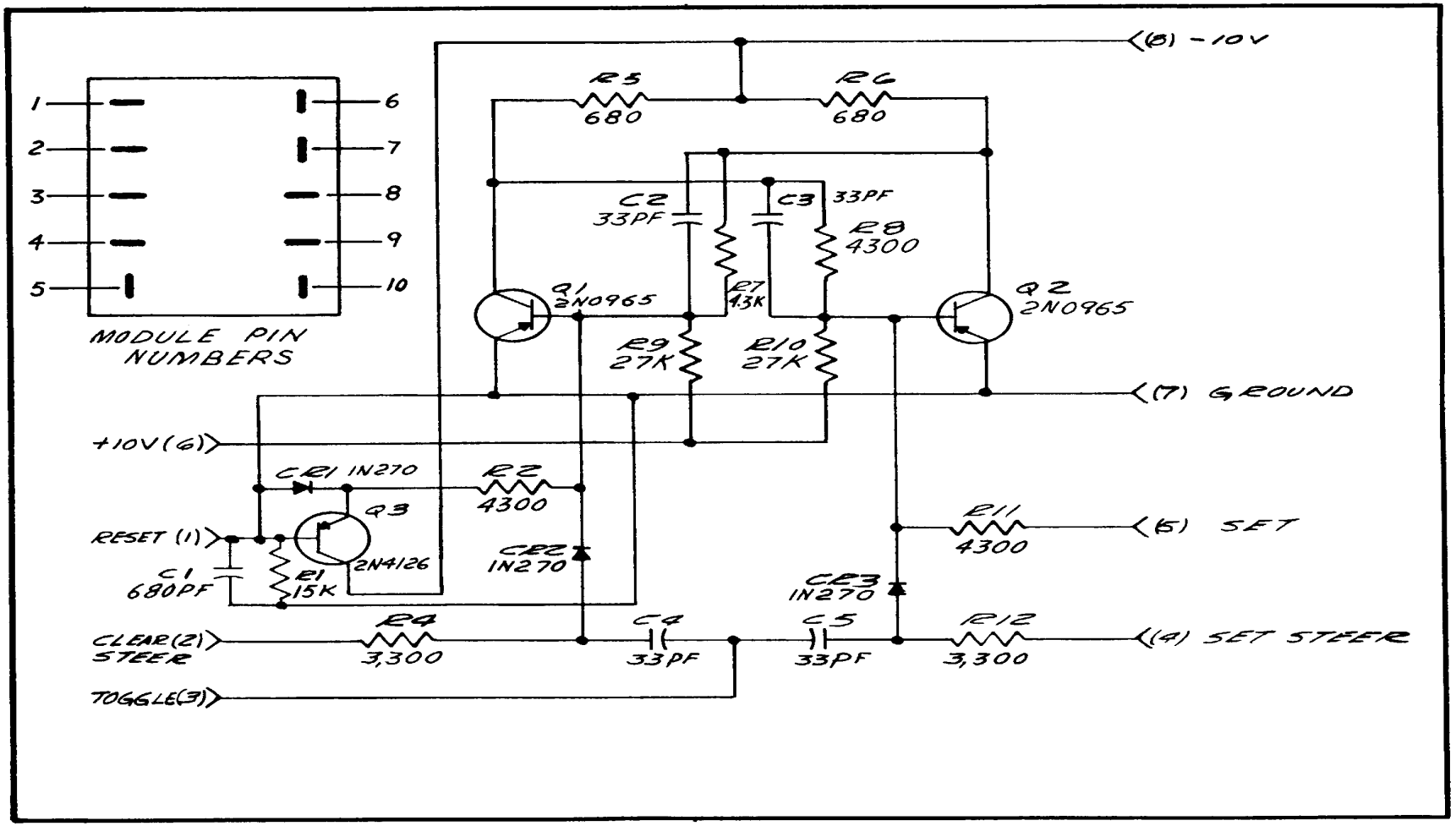


Figure 8-9. Module Assembly, Buffered Reset Lines (CSR-M3).

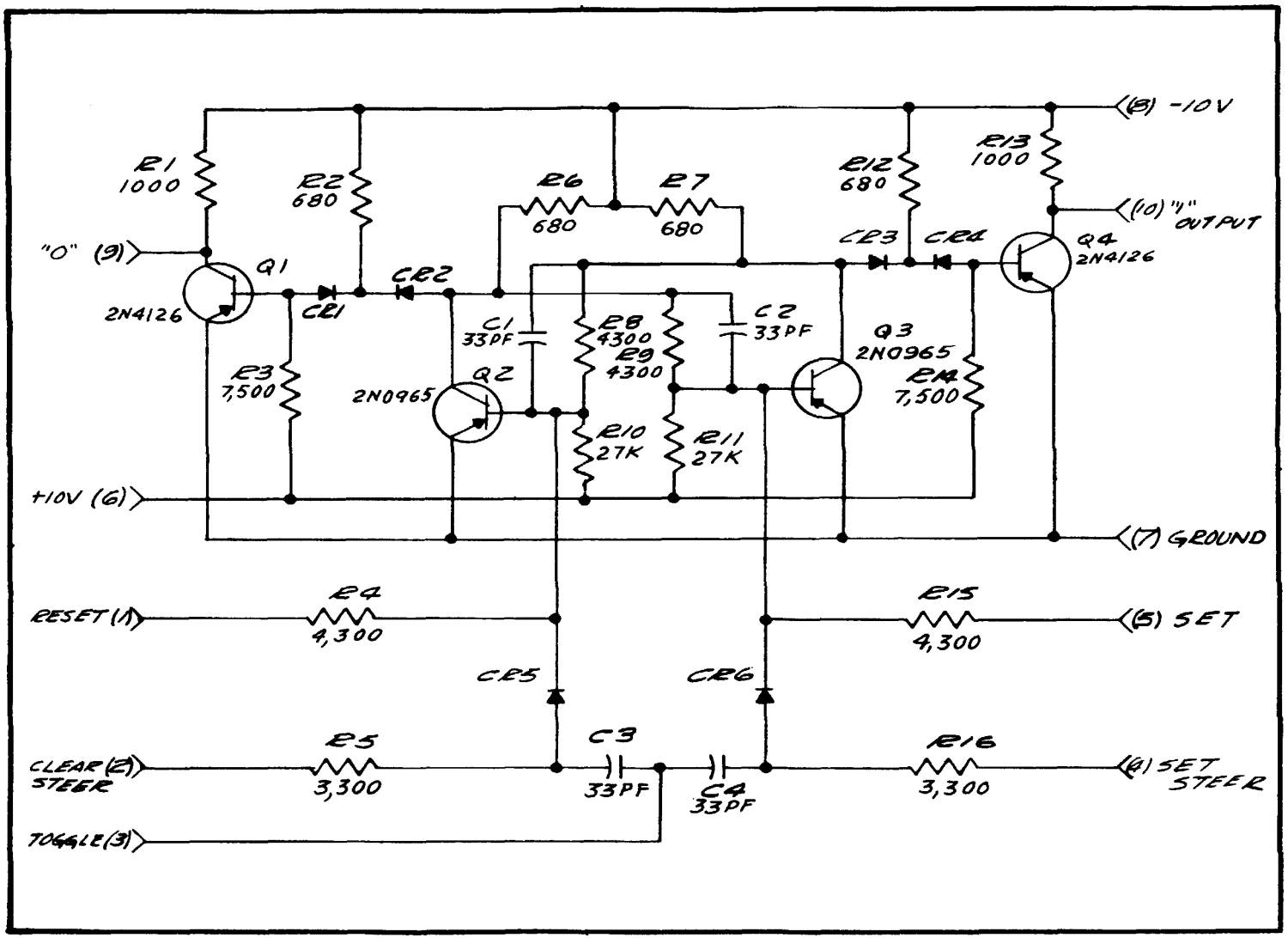


Figure 8-10. Module Assembly, Buffered Output (CSR-M4).

SECTION IX

TIP RING SLEEVE JACK OPTION

9-1. BAUD RATE SWITCH

Data Transmitters containing the Tip Ring Sleeve option (TRS) will have the BAUD RATE switch changed as follows:

Position	Baud Rate (old)	Baud Rate (new)
1	45.50	45.50
2	50.00	74.20
3	55.60	96.00
4	61.12	61.12
5	75.00	37.5

Note
Refer to figure 9-1 for wiring changes to BAUD RATE switch S2.

9-2. TIP RING SLEEVE JACK OPTION

Refer to figure 9-2 for wiring modifications made for the TRS Jack option.

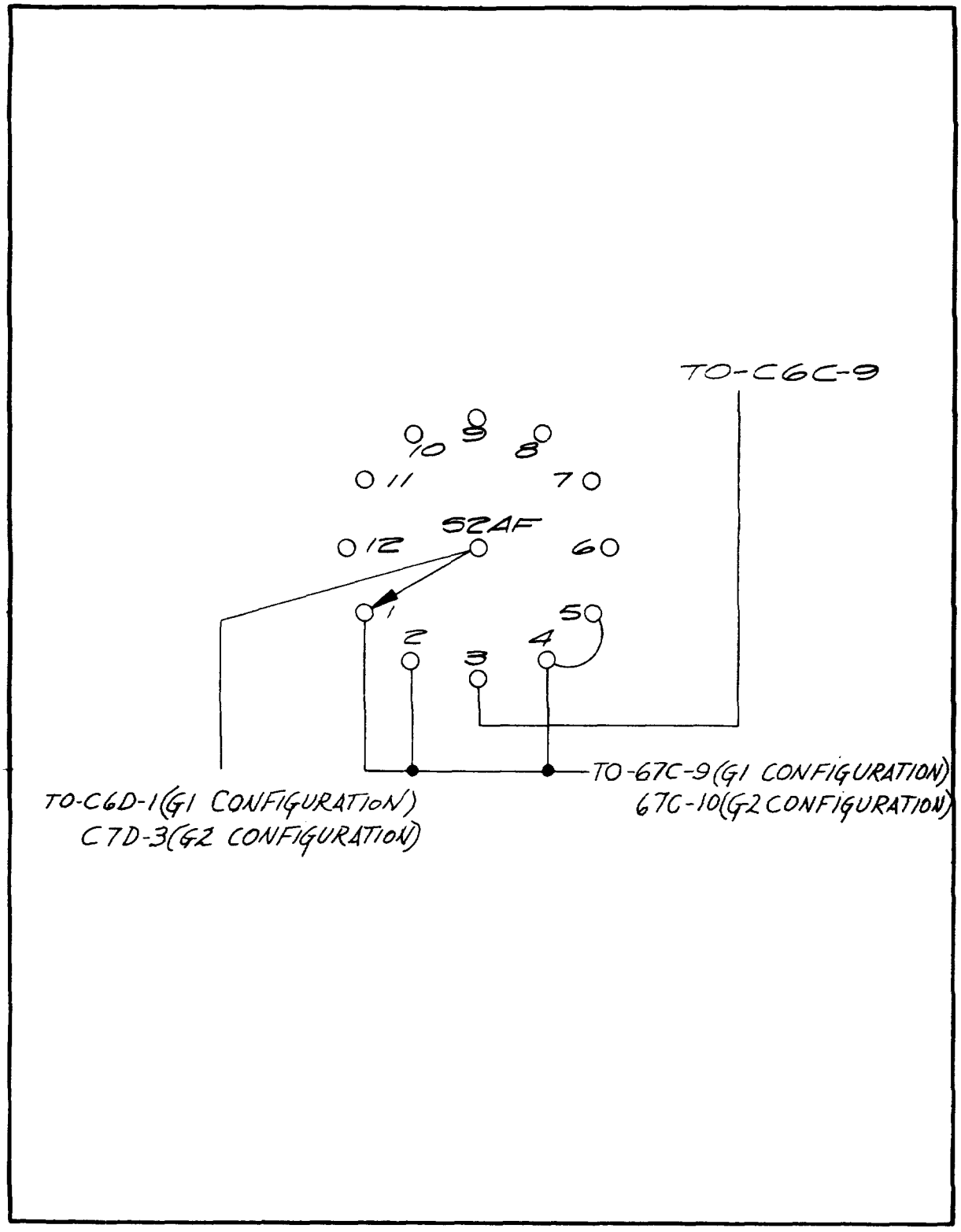


Figure 9-1. BAUD RATE switch S2, wiring for TRS Option.

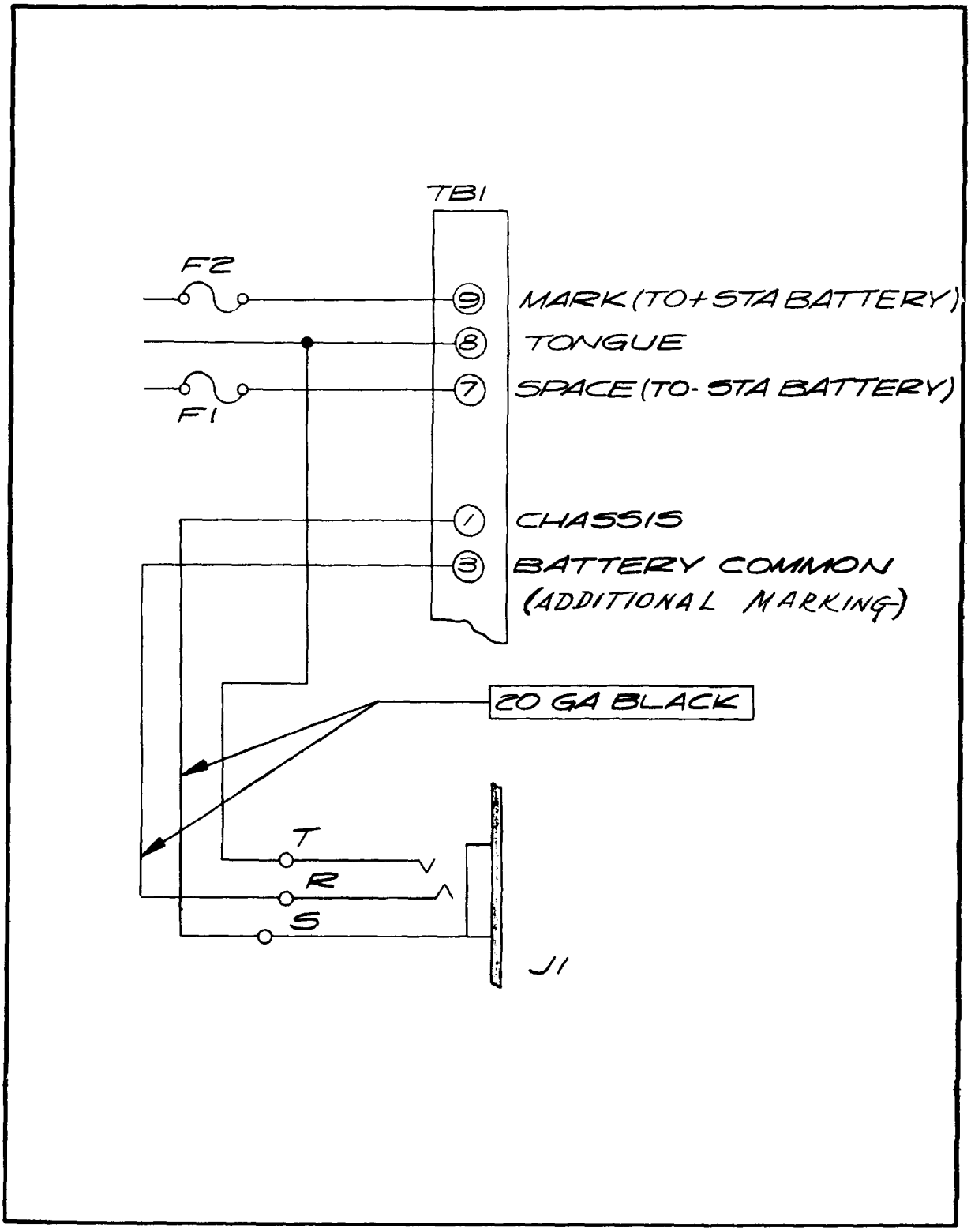


Figure 9-2. TRS Jack Wiring Modifications.

PART B

SECTION I

INTRODUCTION

1-1. GENERAL

The Data Analyzer, Model 7422 (figure 1-1), is a solid-state unit designed to measure telegraph signal distortion. Digital techniques are used to in sure reliable and accurate operation, without maintenance, for long periods of time.

Fundamentally, telegraph distortion measurement is one of time-interval measurement. Time, between transitions of the input signal, is measured and the deviation from the ideal or anticipated time interval is expressed as percent distortion. The method of measurement and analysis is discussed in detail in Section IV, Principles of Operation.

The Analyzer monitors data telegraph signals in either start/stop or synchronous mode, and operates at signal rates from 45.5 to 9600 bauds. It compares the monitored signal with a synchronized time base and displays the percent of signal distortion on a meter and provides the signal for oscilloscope display. Outputs for driving the monitor oscilloscope (which contains its own circuits) are taken from connector J3 on the rear panel of the Analyzer. Early, late and input indicator lamps are provided on the Analyzer panel.

Both high and low-impedance telegraph signals are sampled at selected amplitudes of current and voltage. Mark-to-space (M/S) and space-to-mark (S/M).

transitions are converted into pulses for control of the digital distortion measuring circuits of the Analyzer.

High-frequency noise and transient pulses are stripped from the digital data (when so desired) by switching an RC filter into the data stream ahead of the threshold detector.

The telegraph signals are applied to the Analyzer circuits through either LO-Z or HI-Z telephone input jacks.

CAUTION

Insertion of excessive dc voltages into the H1 Z input jack, due to improper connections at the dc patch boards, will cause excessive damage to modules.

1-2. DATA ANALYZER CHARACTERISTICS

The Data Analyzer, Model 7422, characteristics are listed in table 1-1.

Figure 1-1. Data Analyzer Model 7422 (Front View)

Table 1-1. Data Analyzer, Model 7422 Characteristics

Distortion Type Measurements	1. Total peak 2. Early peak 3. Late peak 4. Average 5. Marking bias 6. Spacing bias 7. Marking end 8. Spacing end 9. Fortuitous 10. Characteristic 11. Cyclic 12. Speed
Distortion Readout	Distortion measurement is displayed on an easy-to-read front-panel meter calibrated from 0 to 50% in 1% increments. Meter may be connected to remote locations. Timing of the measured transition (i.e. early or late) is indicated by two front panel lamps.
Distortion Accuracy	Distortion accuracy is ± 1% after one (1)
Peak Distortion	The meter displays the maximum deviation of the selected transition (any transition for total peak) from its correct time position.

Table 1-1. (Continued)

Measurement Selection	Front panel control permits measurement of a specific transition or all transitions of 5 to 14 unit codes (7 to 16 unit intervals per-character) for start-stop signals. A front panel start-stop/synchronous switch permits determination of early or late transition timing and percent distortion for all synchronous codes. Space-to-mark and mark-to-space transitions are measured independently.
Meter Reset	A three-position switch marked "off", "auto", and "manual" controls resetting of the percentage distortion meter. The automatic reset position resets the meter at approximately 4.5-second intervals.

Table 1-1. (Continued)

Indicator Lamps	Two front panel lamps indicate early or late transitions. Another front panel lamp indicates when the input is on steady mark, steady space, or keyed.
Temperature	Analyzer Model 7422 operates as specified over the temperature range from 0 degrees to 50^{o} C with a relative humidity of 95%.
Internal Speeds	Timing signals for the DAS-10 system originate within Model 7422 Analyzer enclosure. Digital techniques used in the Model 7422 Analyzer result in accuracy independent of baud rate. Any baud rate may be accommodated up to 9600 bauds. Front panel switch is provided to select any of the following twelve (12) rates: 9600, 4800, 2400, 1200, 600, 300, 150, 75, 61.12, 55.60, 50.00 and 45.50.

Table 1-1. (**Continued)**

	The four lowest modulation rates above may be conveniently changed by patch plug, eliminating the need to purchase, and stock extra modulation rate printed circuit cards.
	Front panel switch permits selection of the 12 crystal-controlled rates as described above. Clock accuracy is 0.0 1 %.
	Variable frequency oscillator in con junction with the rate switch permits operation within all rates indicated from 37.5 baud through 9600 baud. A vernier control allows +10% speed range variation.
	Removable card insert permits modulation rate indications to be changed conveniently. Clock output is avail able at rear.

Table 1-1. (Continued)

	Reference clock phase for synchronous distortion measurements is provided by a phase-lock system. Acquisition time is approximately 5 seconds.
Input Circuits	Neutral 20 MA ± 100/o%;maximum input resistance 300 ohms. Neutral 60 MA ± 10%; maximum input resistance 100 ohms . Polar 20 or 30 MA ± 10%; maximum input resistance 300 ohms. Polar input ± 5V minimum to ± 130V maximum DC; input impedance greater than 50,000 ohms. Return circuit for this input is signal ground. Input circuitry is constructed with plug-in modules which permits special inputs as required.

Table 1-1. (Continued)

	Input filter can be provided (as per customer requirements) for the removal of transient impulses that may be present on extremely noisy lines.
Power Supply	Logic level power (-10VDC and +10 VDC) for the DAS-10 system comes from power supply package in the 7422 analyzer enclosure. AC input to this power supply is 115/230 ± 10%/o VAC 50-400.
Signals Provided for A-Scan Model 7431	Control signals for X, Y, and Z axes of the "A" Scan cathode-ray display originate or are derived from Analyzer Model 7422. They are listed and described in the technical specifications for the A-Scan Model 7431.

Table 1-1. (Continued)

Functional and Physical Characteristics	Analyzer Model 7422 is a functionally independent unit because the time base and power supply are self-contained. It can be used alone for analysis of incoming traffic if observation of waveform and sampling point is not required. Size: 7-inches high standard rack mount, depth approximately 22 inches. Receptacles at rear for connection to A Scan Model 7431 and transmitter Model 7413. Rack Mount Unit Weight is 37-1/2 pounds.

SECTION II

INSTALLATION

2-1. GENERAL

After removal from the shipping carton, inspect the Data Analyzer for possible in-shipment damage. Report all damages in accordance with paragraph 1-3, part A.

2-2. UNPACKING

The Data Analyzer unit is shipped in a re-inforced packing case designed to provide maximum protection during transport and handling. No special instructions are required for unpacking. However, care should be exercised to prevent damage. All parts of the unit should be carefully inspected for possible concealed damage during transit.

2-3. MECHANICAL INSTALLATION

The Data Analyzer is housed in a desk-top package which may be used on any flat surface . The unit may also be rack-mounted by use of a rack-mount adapter kit. Directions for rack mounting are included in the kit, and it is recom mended that the top and bottom covers of the Analyzer be removed to provide additional ventilation when rack mounted.

2-4. ELECTRICAL INSTALLATION

The Data Analyzer operates from either 115 volts or 230 volts, 60 cps to 400 cps.

Before connecting the Analyzer to a power source, remove the top cover of the Analyzer to determine that the 115/230 VAC slide-switch on top of the power supply unit shows the appropriate voltage to accommodate the commercial source. To connect the power source, plug the power cord into the AC outlet.

2-5. INPUT-OUTPUT CONNECTIONS

For input and output connections refer to table 2-1 Input and Output Connections. The connector pins are designated by module, connector board, column, row and pin at the connector board where the cable enters the system. For example: E9A5 designates pin 5 of the module on connector board E in column 9, row A.

2-6. REFERENCE DESIGNATIONS (See figure 2-1)

The reference designation system provides both identification and physical location information for each module, as follows:

A. Designations consist of groups of numbers and letters arranged in an alternating manner so that no two numbers are adjacent, as in 4A5D6B1.

B. No attempt is made in the designation to distinguish a module from its corresponding connector. It is understood, for ex ample, that module D6B plugs into connector D6B.

Table 2-1. Data Analyzer Input and Output Connections

Function	Pin Number	Internal Destination	Frequency
Output Connections			
75 Baud	J2-6	A4C5	7500 cycles
300 Baud	J2-8	A3C5	30 kc
1200 Baud	J2-10	A2C5	120 kc
4800 Baud	J2-12	A1C5	480 kc
Non-Integers	J2-14	A5A10	100 x Baud Rate
150 Baud	J2-25	A4C10	15 kc
600 Baud	J2-27	A3C10	60 kc
2400 Baud	J2-29	A2C10	240 kc
9600 Baud	J2-31	A1C10	960 kc
+10 volts	J2-2		
Signal Ground	J2-4		
Signal Ground	J2-23		
-10 volts	J2-17		
-10 volts	J2-16		
Chassis Ground	J2-19		
Chassis Ground	J2-37		
Output Connections			
Vertical	J3-1 & TB1-1		

Table 2-1. (Continued)

+10 volts	J3-2	
Horizontal	J3-3 & TB2-2	
Transition Sync	J3-4 & TB2-3	
Character Sync	J3-5 & TB2-4	
Blanking	J3-6 & TB2-5	
- 10 volts	J3-7	
- 10 volts	J3-8	
Intensity Markers	J3-9 & TB2-6	
Signal Ground	J3-10	
Chassis Ground	J3-11	
115 volts AC	J3-12	
115 volts AC	J3-13	
115 volts AC	J3-14	
115 volts AC	J3-15	
-Ext. Meter	TB2-9	
+Ext. Meter	TB2-10	
Input Connections		
Ext. Clock	J1	BNC Connector
High Z In	TB2-1	
Low Z Tip	TB2-3	
Low Z Sleeve	TB2-4	
Signal Ground	TB2-11	
Chassis Ground	TB2-12	

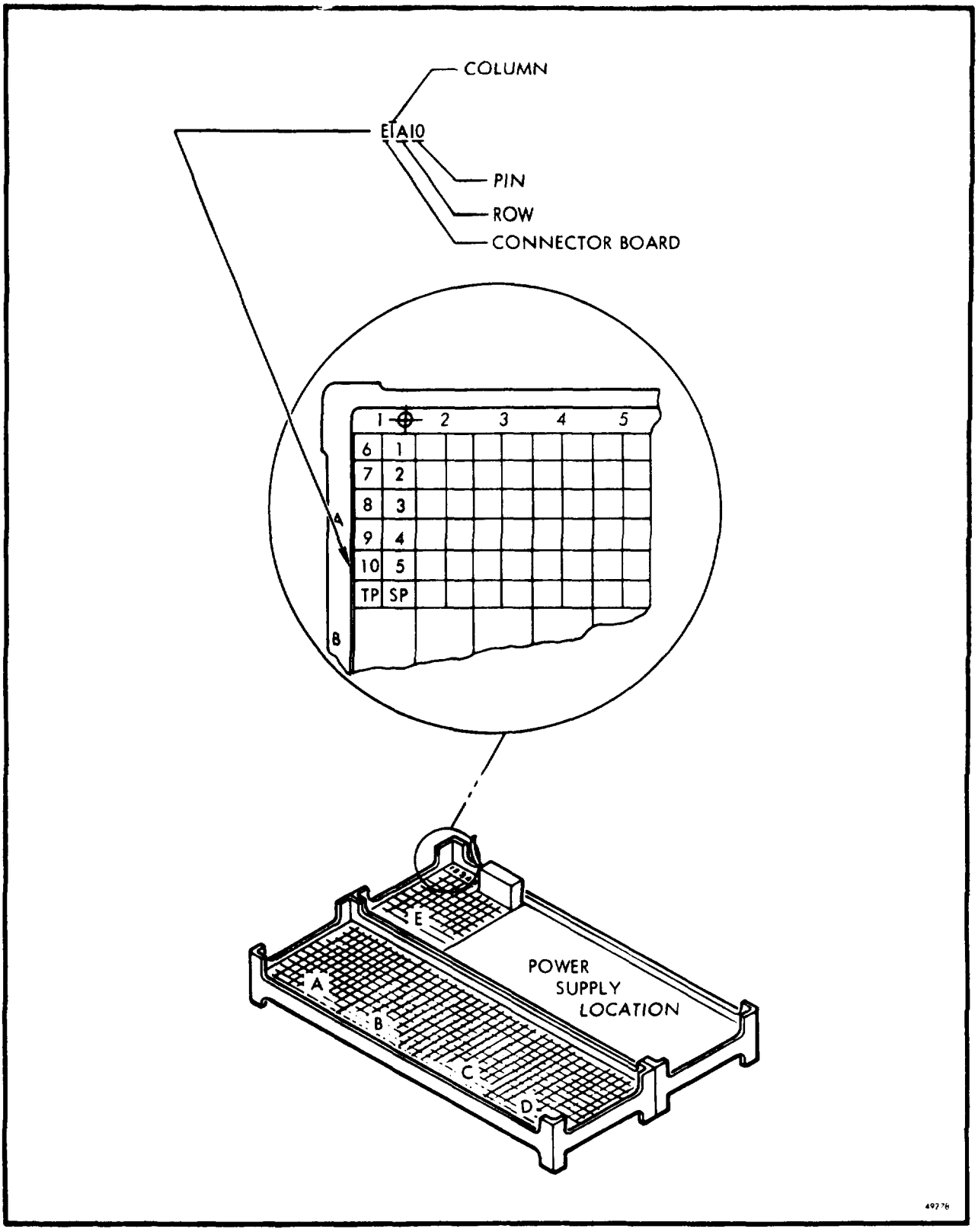


Figure 2-1. Reference Designations

C. Reference designations for modules do not contain circuit function nor circuit name information. The module name and part number is assigned on drawer assembly drawings or in logic diagrams. The circuit function is also illustrated schematically on logic diagrams.

2-7. MODULE DESIGNATIONS (See figure 2-1)

Modules may be mounted in either vertical or horizontal assemblies. In either case, the basic building block is a frame which accepts four 50 module connector boards. Boards are lettered A, B, C, etc., omitting letters which might be confused with numbers.

Individual module connectors on the board are arranged in a black and-white checkerboard fashion so that module locations are clearly defined.
The module location (connector) is identified by its row and column location on the board.

Numbers cast along the top and bottom edges of the frame identify module connector columns (1 through 10) of each board. Letters A through E, cast along the sides of the frame, identify the module connector rows. A module is identified by its board, column, and row position in that order. A3C, for example, identifies a module location on board A, column 3, row C.

Individual pin numbers are not marked, but are assigned numbers 1 through 10. The two remaining pins are used as a test point and a component tie-point if desired.

Identification of a single pin, anywhere in the System, is provided by a series of numbers and letters consistent with the pin location, connector board and module connector row and column. For example: the numbers C10A5 indicates pin number 5 of module 10A (column 10, row A) on connector board C. Modules are keyed so they cannot be inserted up side down.

2-8. POWER DISTRIBUTION

Most modules use identical pins to accept power. These are pins 6, 7 and 8 for +10 volts, ground and - 10 volts respectively. "Push-on" jumper strips are frequently used to distribute power along rows of modules.
These are not designated by number but are illustrated in jumper assembly drawings.

2-9. POWER SUPPLY (See figure 2-2)

The Model 58228A Power Supply provides the necessary plus and minus 10 volts for Radiation Digital Logic Modules and other additional circuits. The power supply is designed specifically to mount in a module frame. It mounts in the same space normally required for three contact boards. The over-all height of the mounted power supply is less than 3.5 inches.

For the output voltages, externally-mounted regulator modules are required. These are; Regulator No. 508436 for +10 volts, -10 volts and 9 volts isolated. The -5 volts for D/A Converter modules is supplied by Regulator No. 508367G1. The -10 volts regulator module acts as a drive stage for a high-power series transistor mounted in a heat-sink on the power supply chassis.

Conversion from 115 VAC to 230 VAC is accomplished by a slide switch which is recessed in the top of the power supply to prevent accidental operation. The input to the power supply is fused. The +10 volts can with stand a sustained short circuit, the -10 volts supply has a built-in thermal circuit breaker. A low-noise blower is mounted within the supply to maintain proper air circulation, and over-temperature thermal cut-out is provided. All semiconductors are silicon. A detachable grounding type line cord is provided.

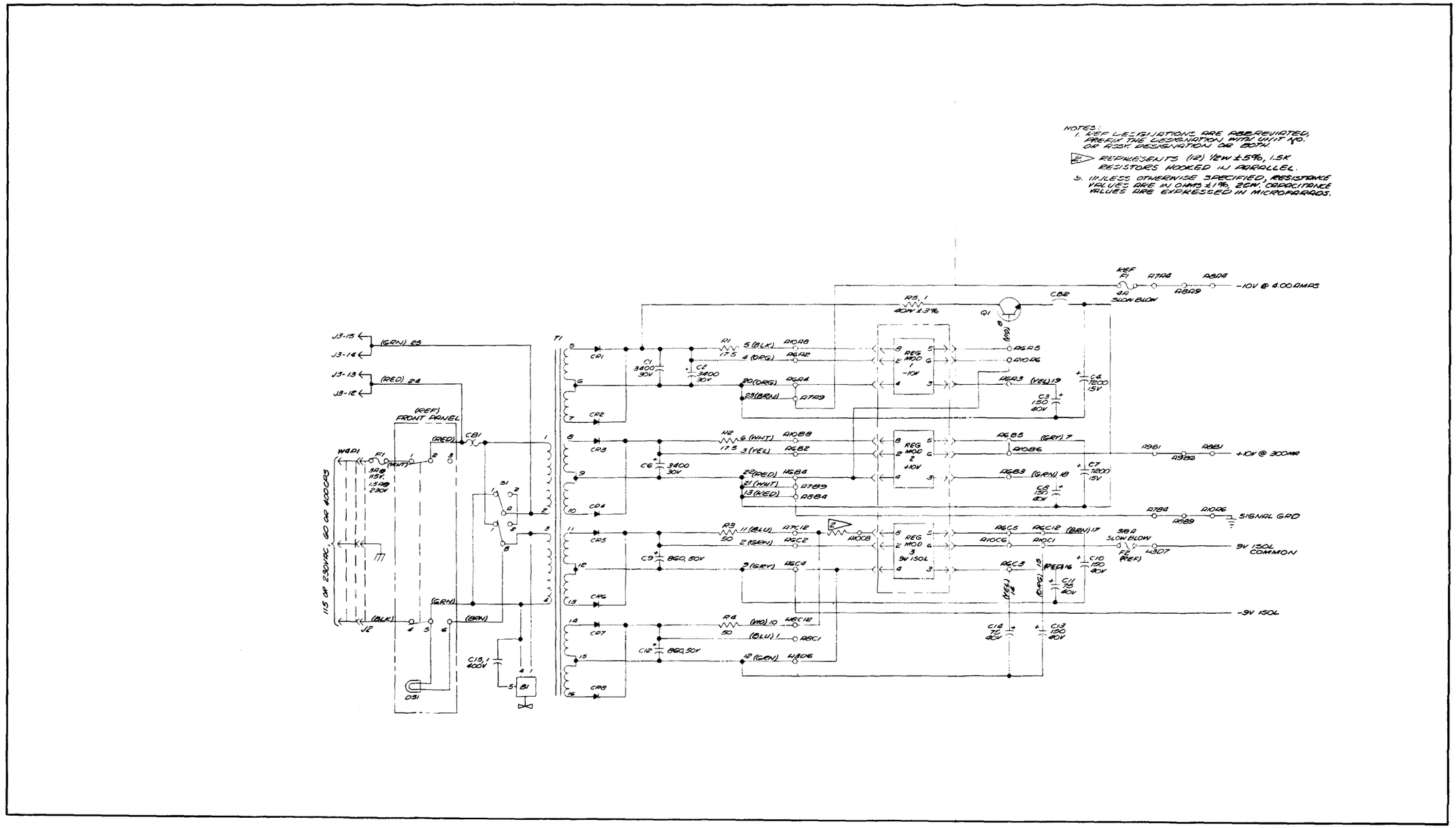


Figure 2-2. Power Supply, Model 58228A

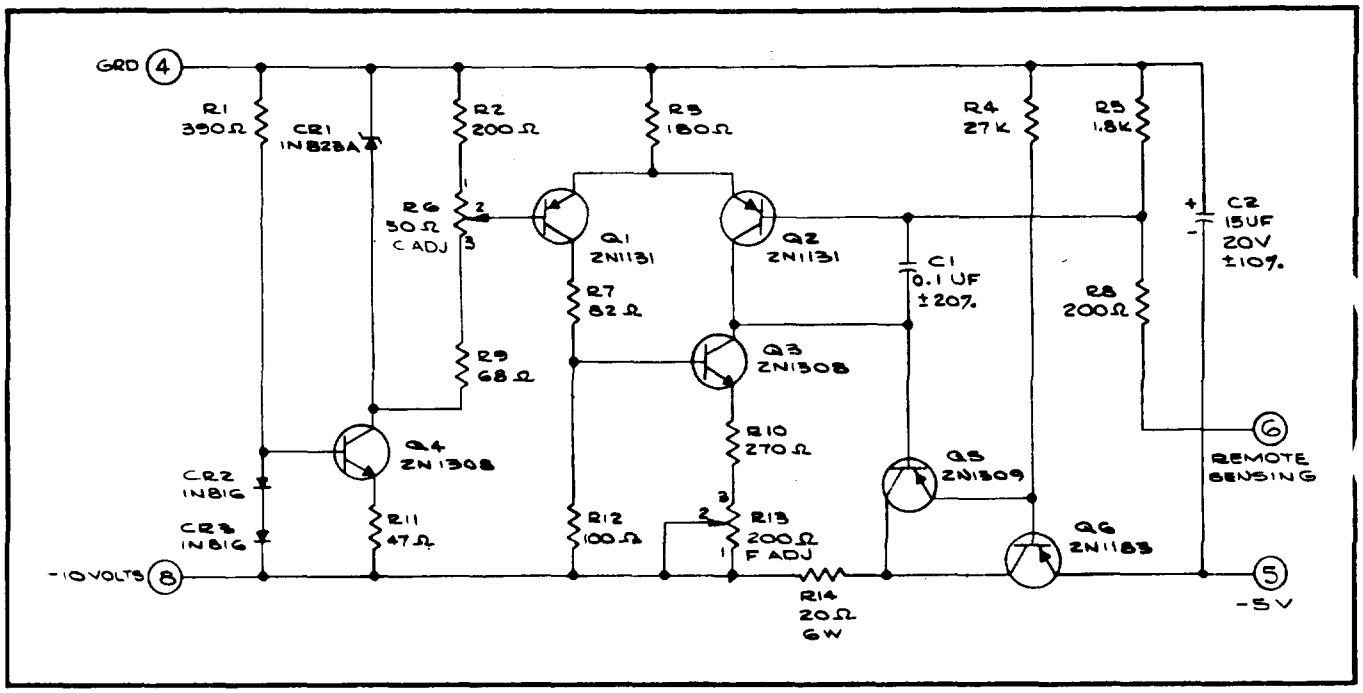


Figure 2-3. -5 Volts Regulator Module

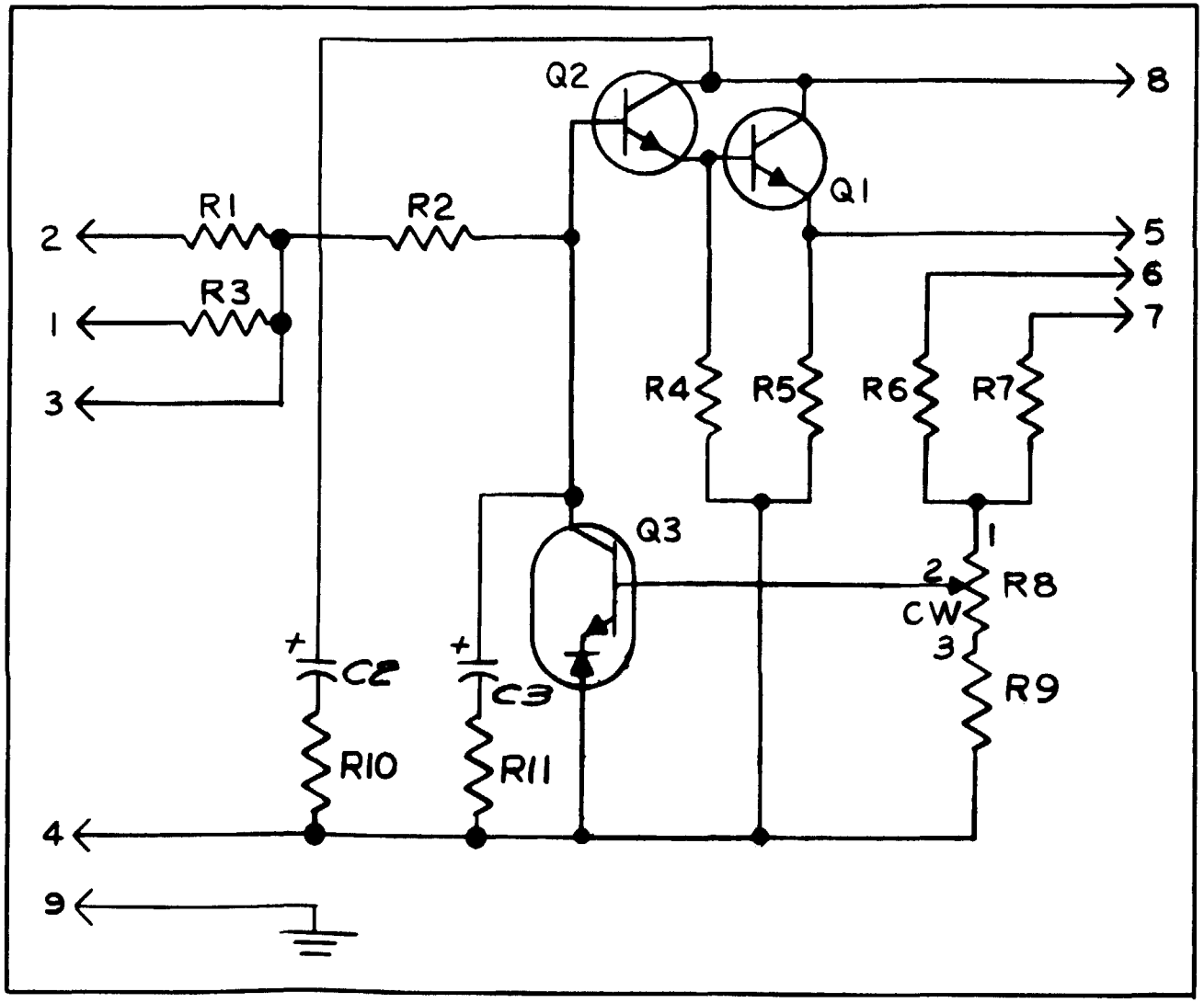


Figure 2-4. (+) and (-) 10 Volts and Isolated 9 Volts, Regulator Module - 508436

SECTION III

OPERATING PROCEDURES

For operating procedures refer to PART A, SECTION III, AND SECTION V paragraph 5-4; also to PART B, SECTION IV for action of controls and indicators.
The Data Analyzer illustrations are in this PART B, SECTION III, Figures 3-1, 3-2 and 3-3.

CAUTION

Insertion of excessive dc voltages into the HIGH Z INPUT Jack, due to improper connections of the dc patch boards, will cause excessive damage to modules.

Rapid rotation of switches will cause damage to internal switch contacts.

Changes to internal programming of the Data Analyzer may cause excessive damage to modules.

Figure 3-1. Data Analyzer, Controls and Indicator (Front View)

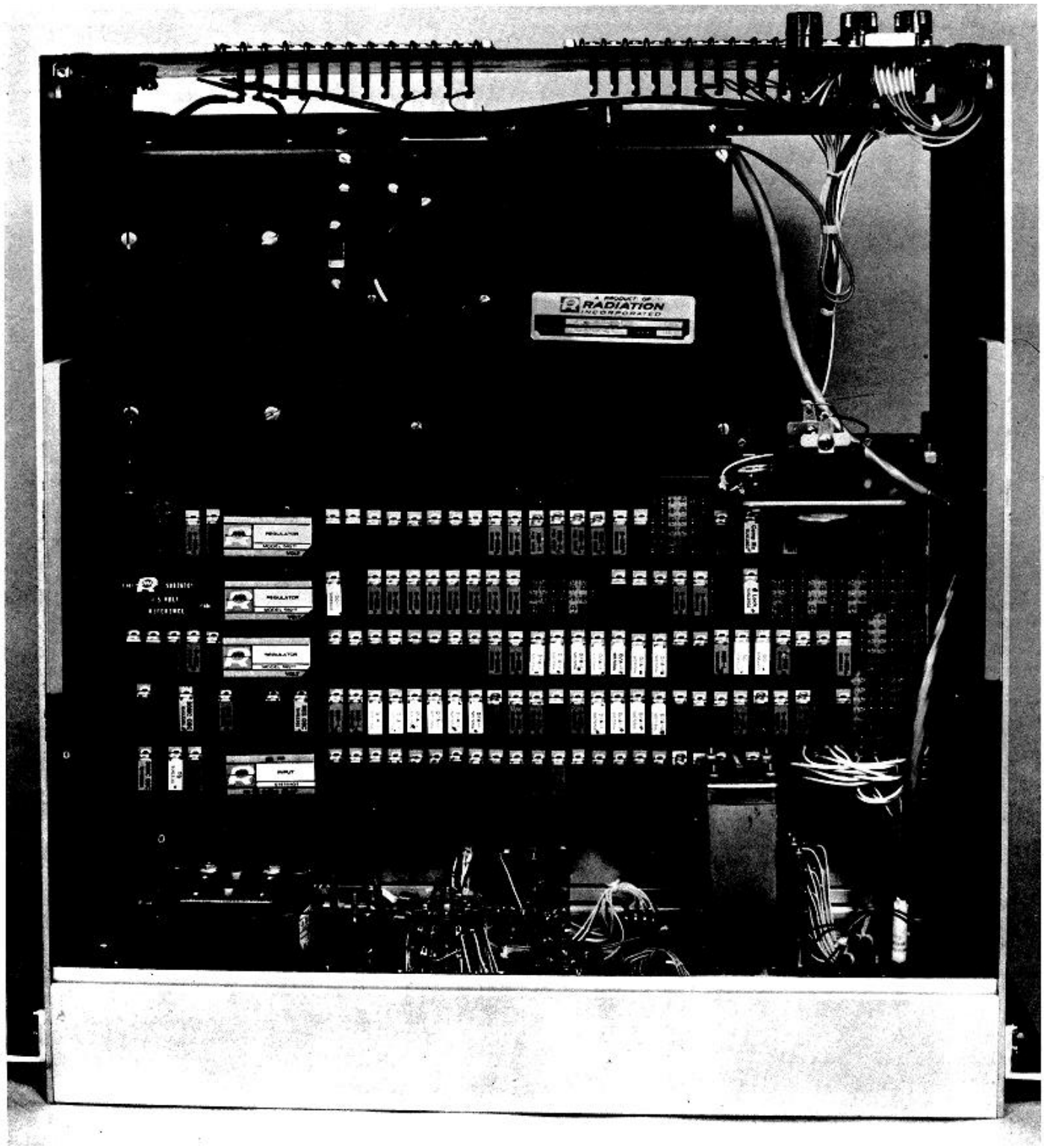


Figure 3-2. Data Analyzer, Controls and Indicators (Top View)

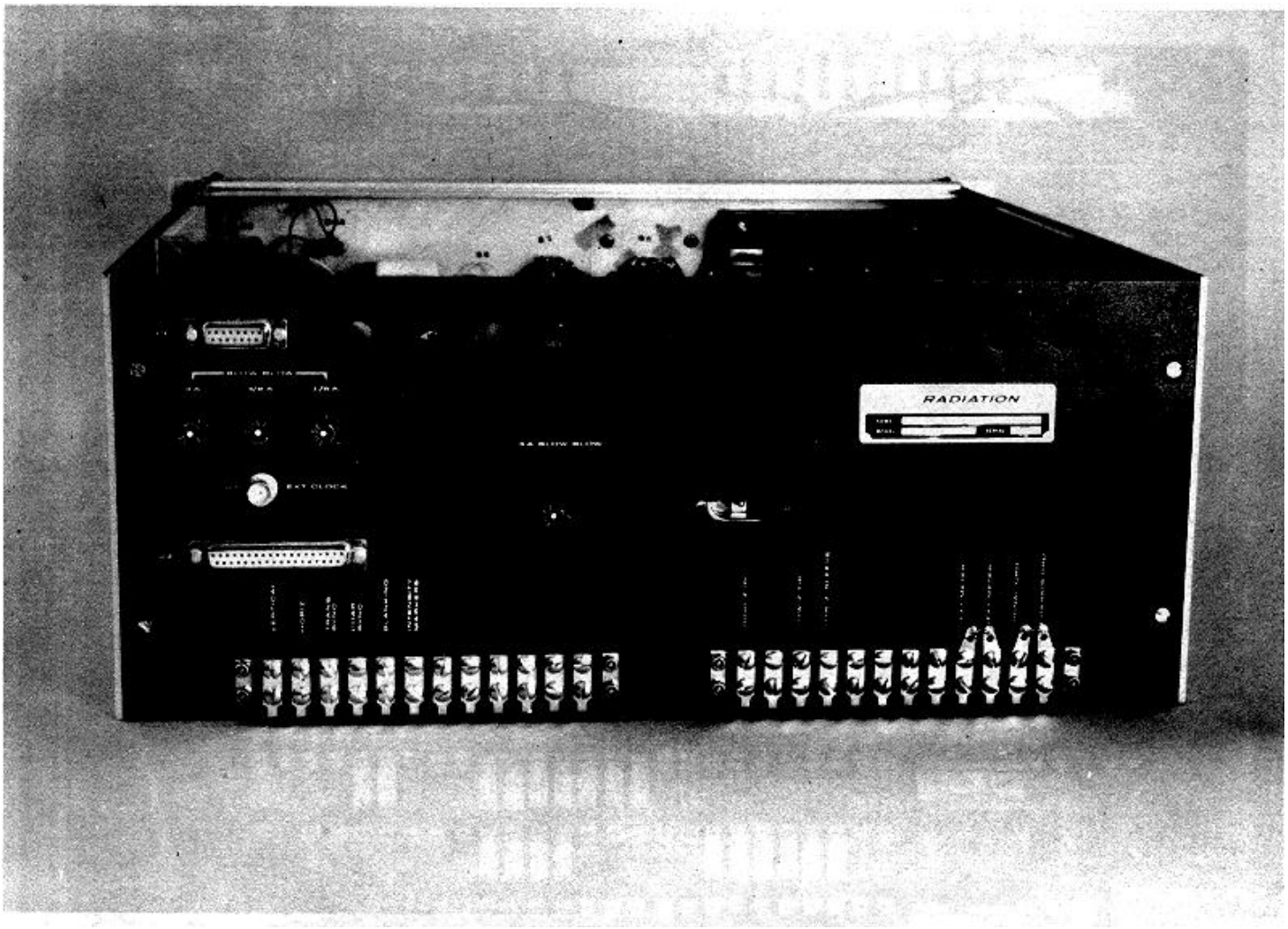


Figure 3-3. Data Analyzer, Controls and Indicators (Rear View)

SECTION IV

PRINCIPLES OF OPERATION

4-1. GENERAL

The Data Analyzer functional block diagram (figure 4-1), logic diagram (figure 4-2) and waveforms (figure 4-3) are used as references in the following discussions:

For Start/Stop operations the timing source is determined by the CLOCK SELECT switch. This permits the operator to select either internal 3.84 megacycle crystal-oscillator, internal variable-frequency oscillator, or external clock input. In synchronous mode the timing source is a voltage-controlled oscillator operating phase-locked to the incoming bit rate.

The clock divider is a 10-stage binary counter using CSR-M1 modules connected for counter applications. When operated as a straight divider binary chain, baud rates 37.5, 75, 150, 300, 600, 1200, 2400, 4800 and 9600 are available. Other baud rates, which do not bear binary relationship to 75 bauds, are accomplished by programmed presetting of the clock-divider chain. Output from the clock divider is a frequency equal to 100 times the selected baud rate.

The output of the clock divider is fed to a 0-50-0 up/down counter which completes one cycle, from 0 to 50 and then back to 0, during one bit period at the selected baud rate. In start/stop operation the character-length counter holds the up/down counter at 0 during the stop pulse and releases it to start counting up at the arrival of the stop/start transition.

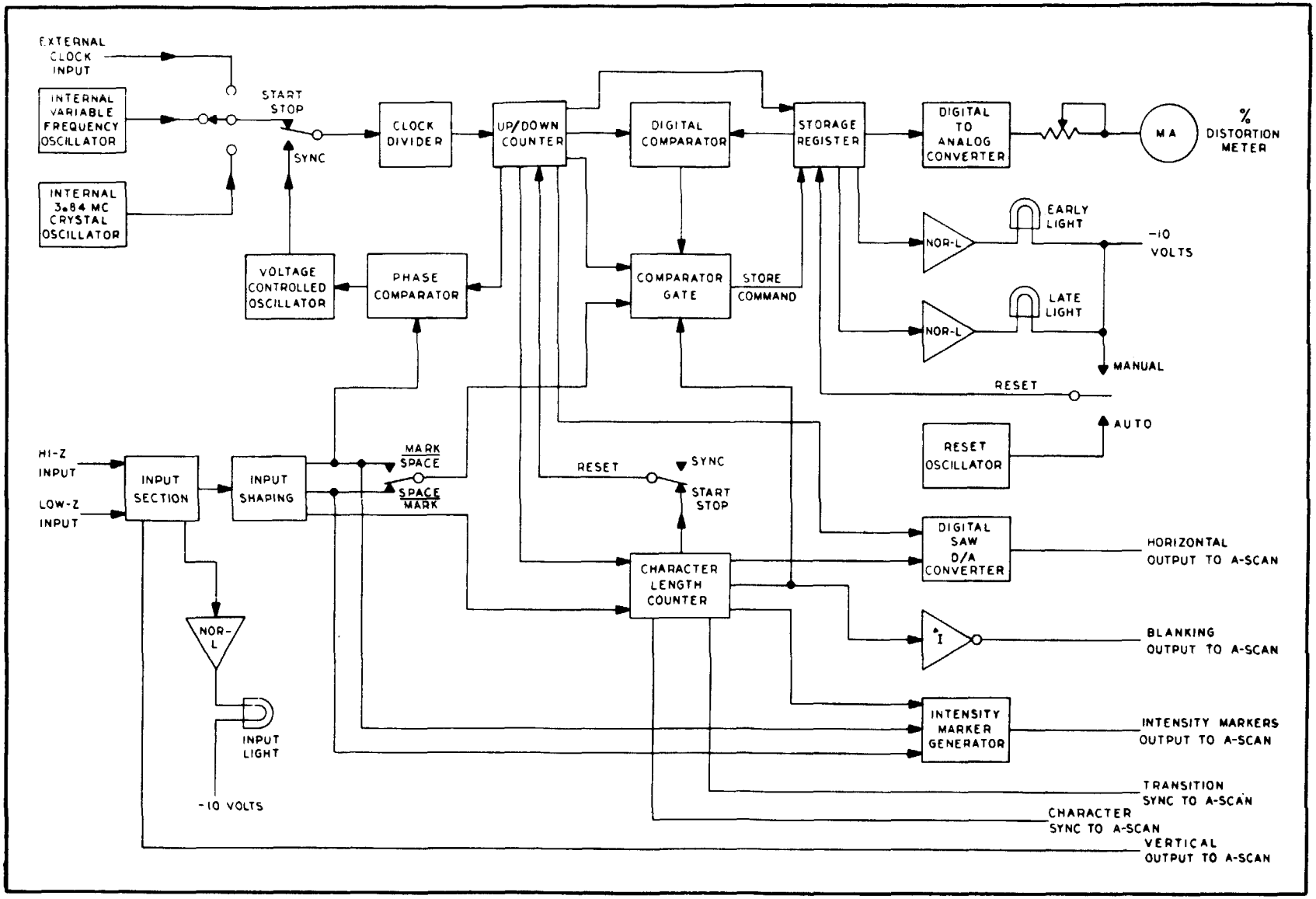


Figure 4-1. Data Analyzer, Block Diagram

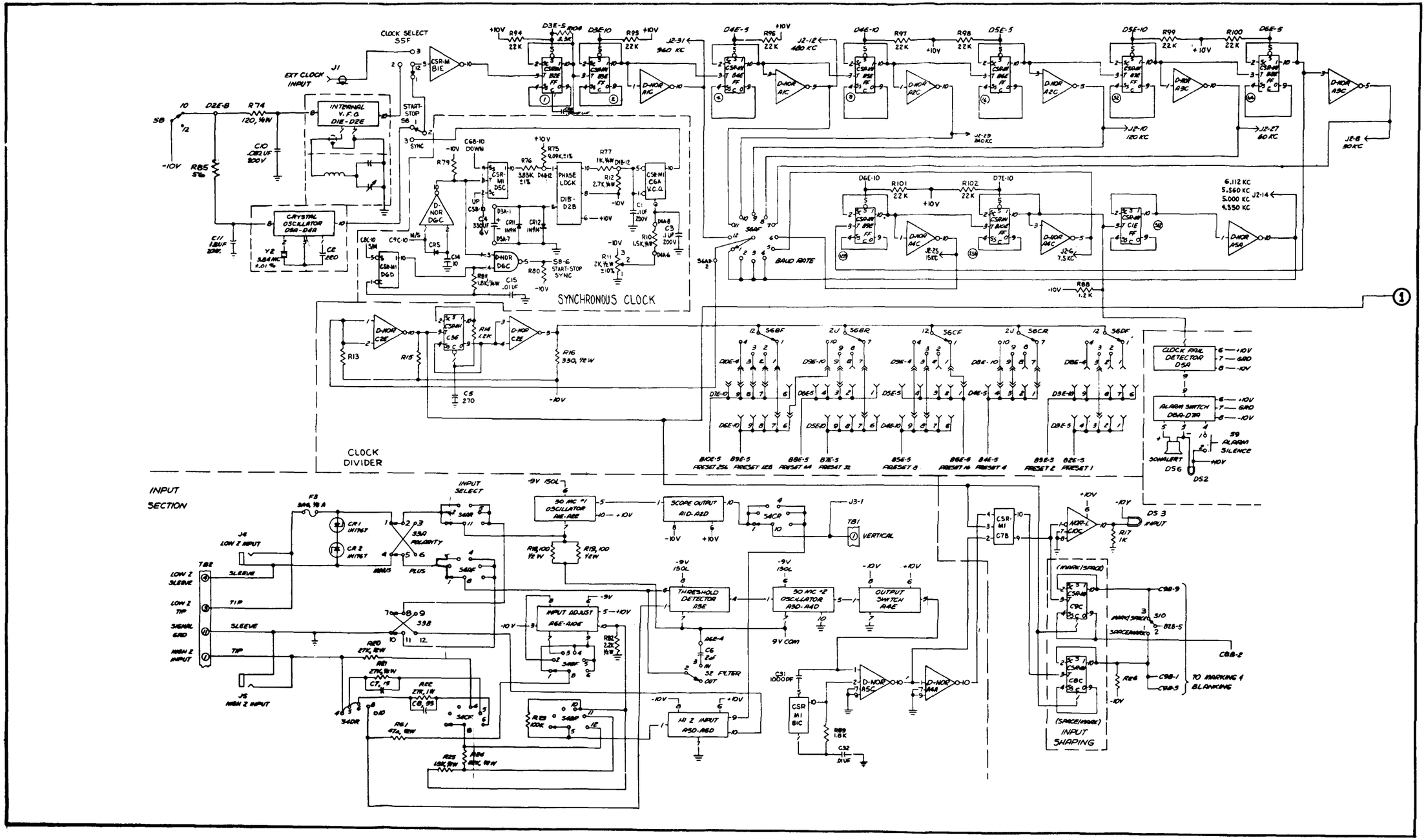


Figure 4-2. Data Analyzer, Logic Diagram G3 Assembly Sheet 1 of 2

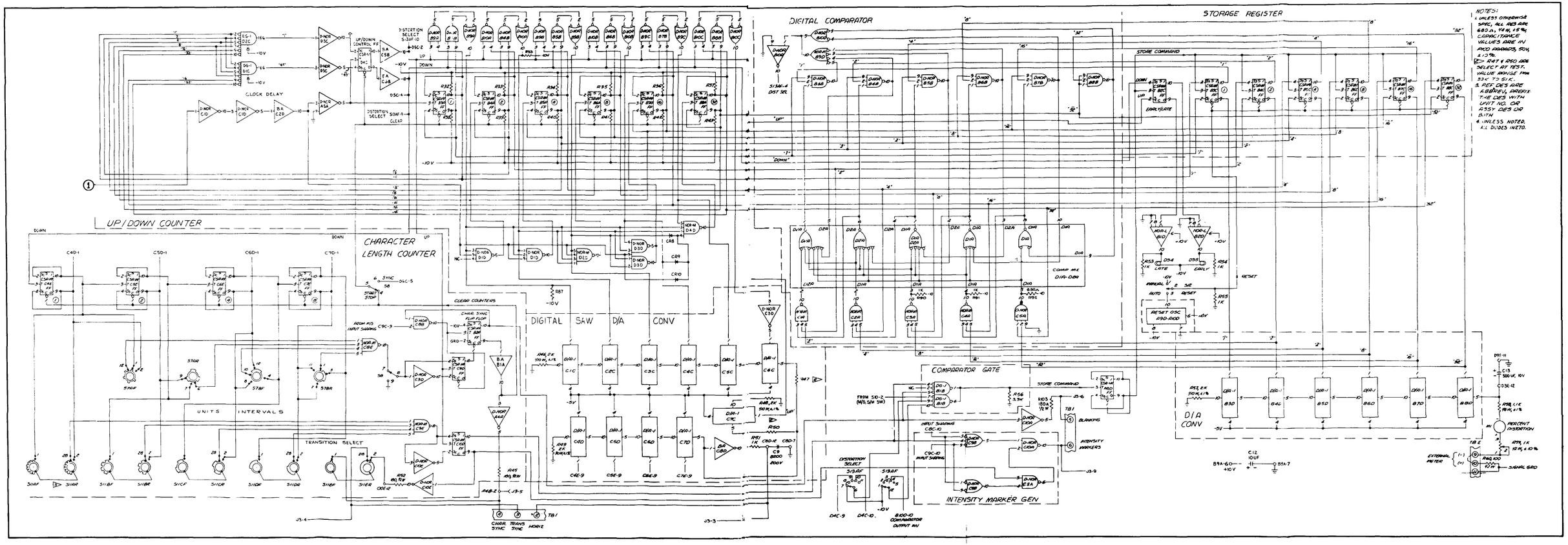


Figure 4-2. Data Analyzer, Logic Diagram G3 Assembly Sheet 2 of 2.

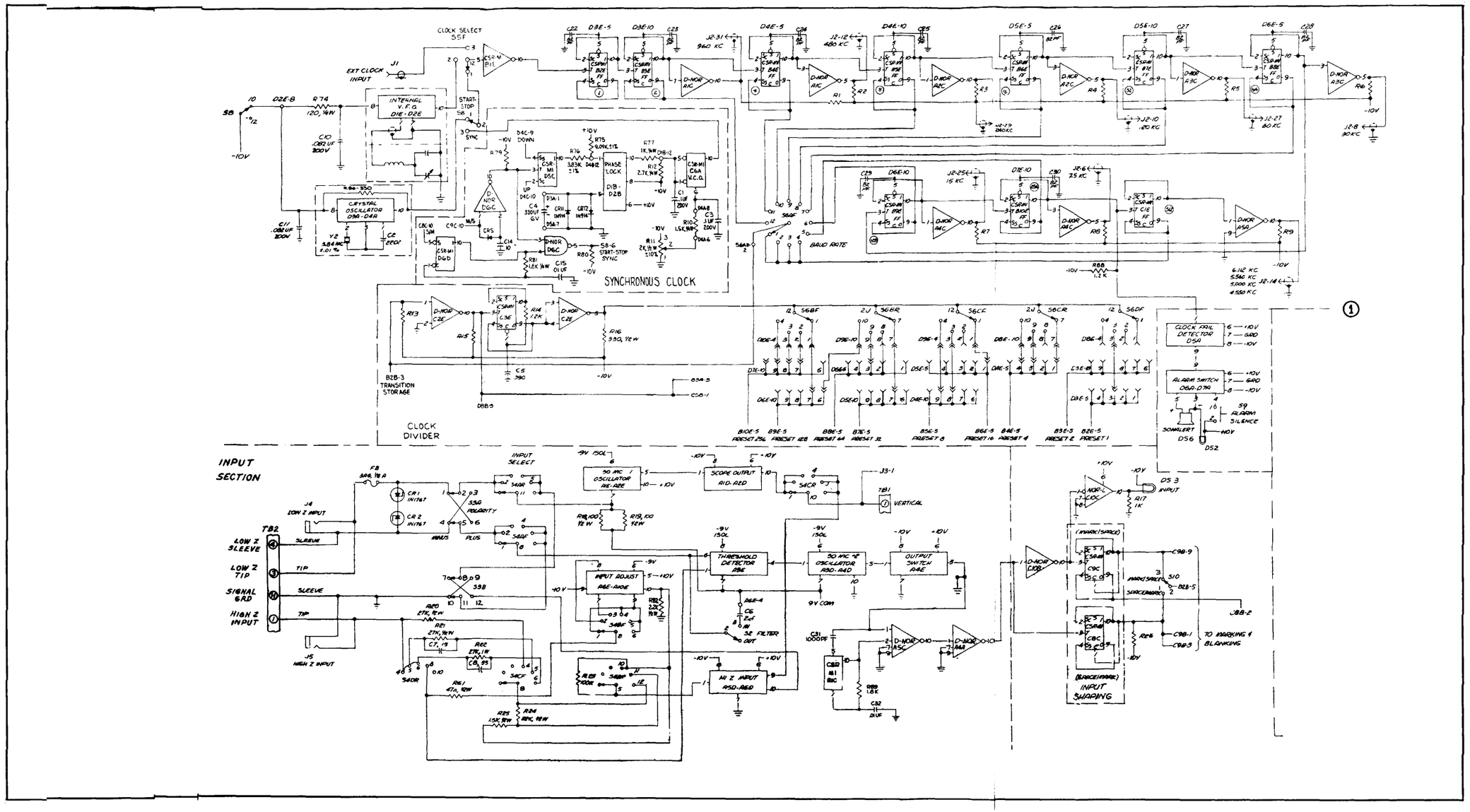


Figure 4-2A. Data Analyzer, Logic Diagram G2 Assembly (Sheet 1 of 2).

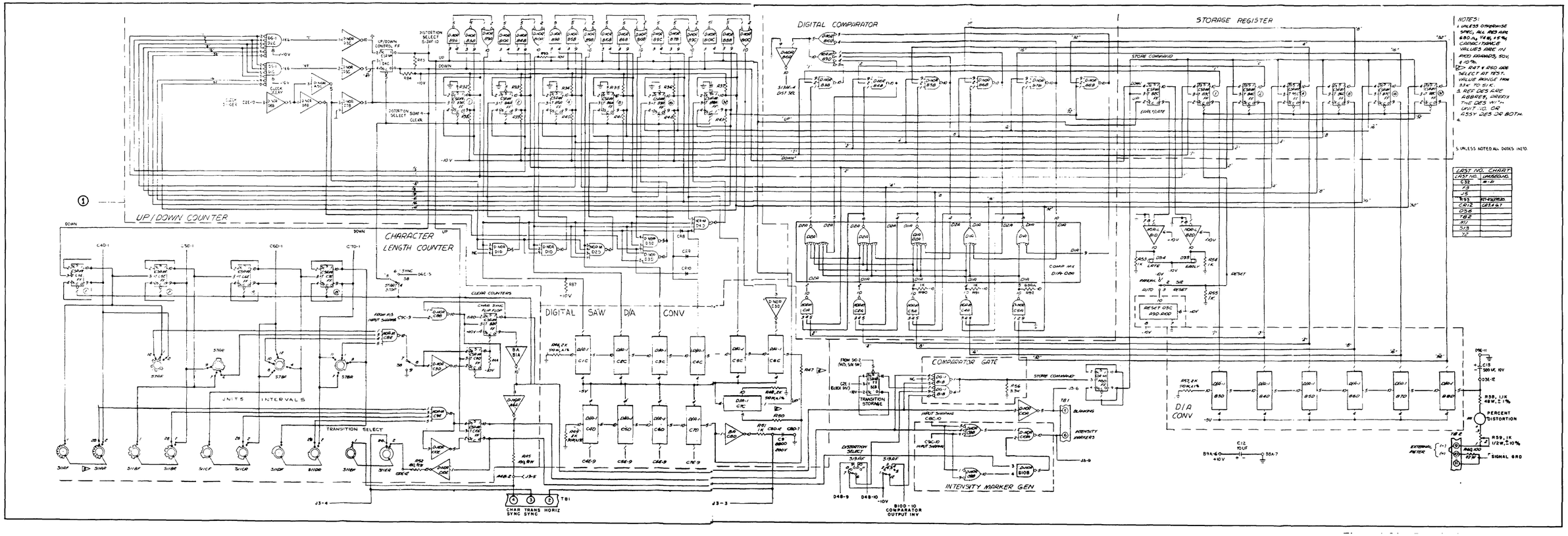


Figure 4-2A. Data Analyzer, Logic Diagram G2 Assembly (Sheet 2 of 2)

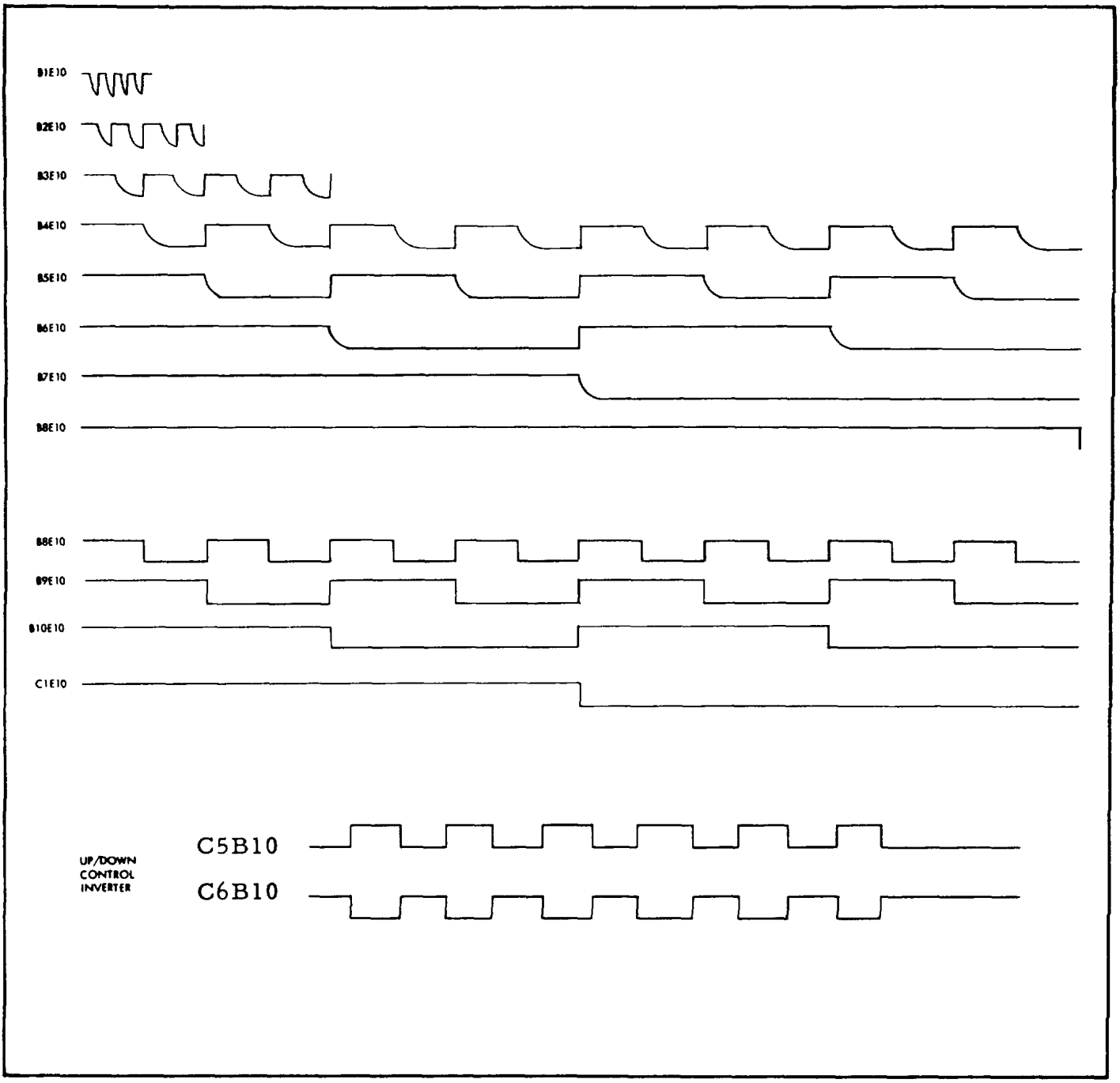


Figure 4-3. Data Analyzer, Waveforms (Sheet 1)

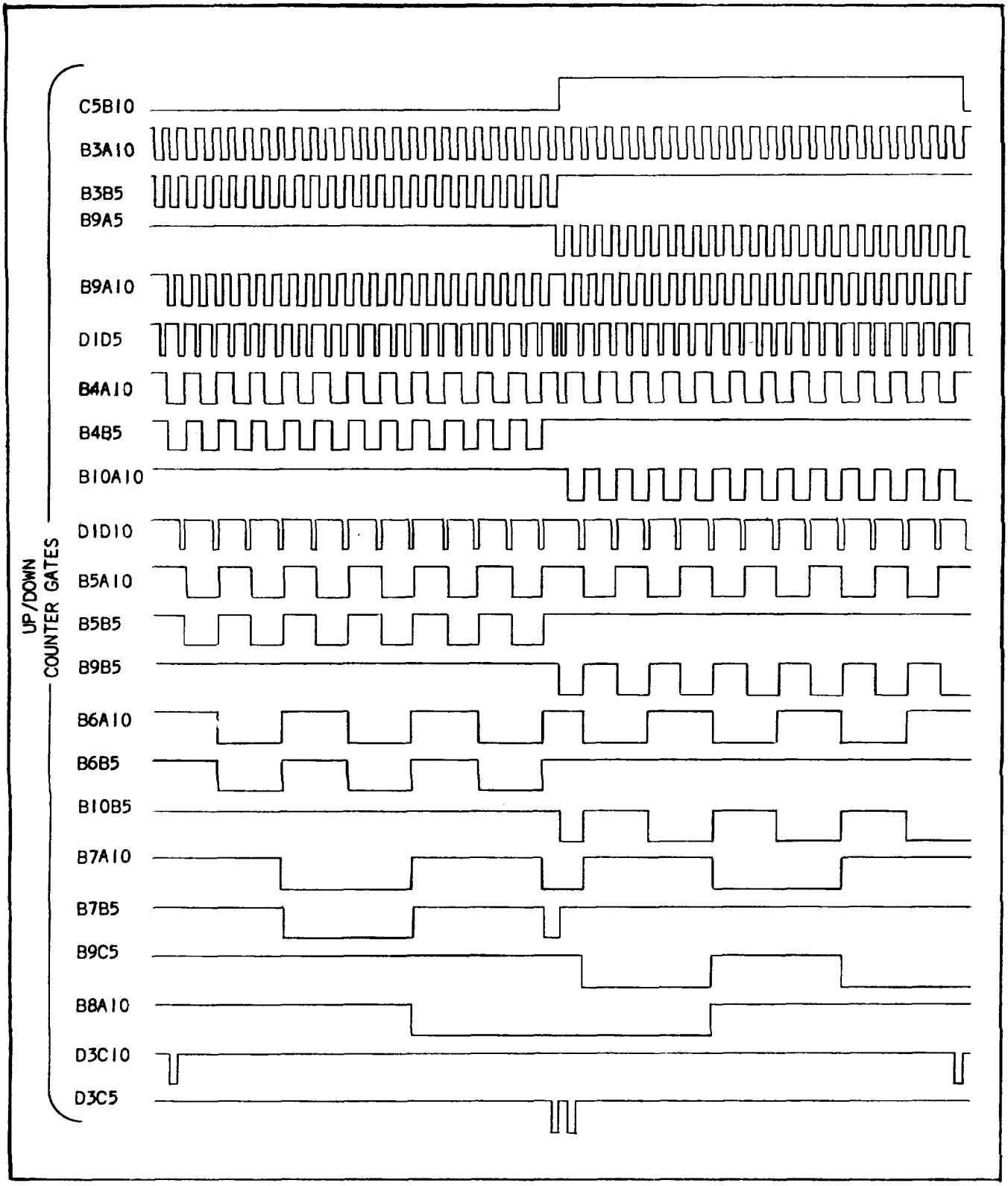


Figure 4-3. DATA ANALYZER, WAVEFORMS (SHEET 2)

CHARACTER LENGTH COUNTER WITH UNITS INTERVALS SWITCH SET FOR 7 UNITS

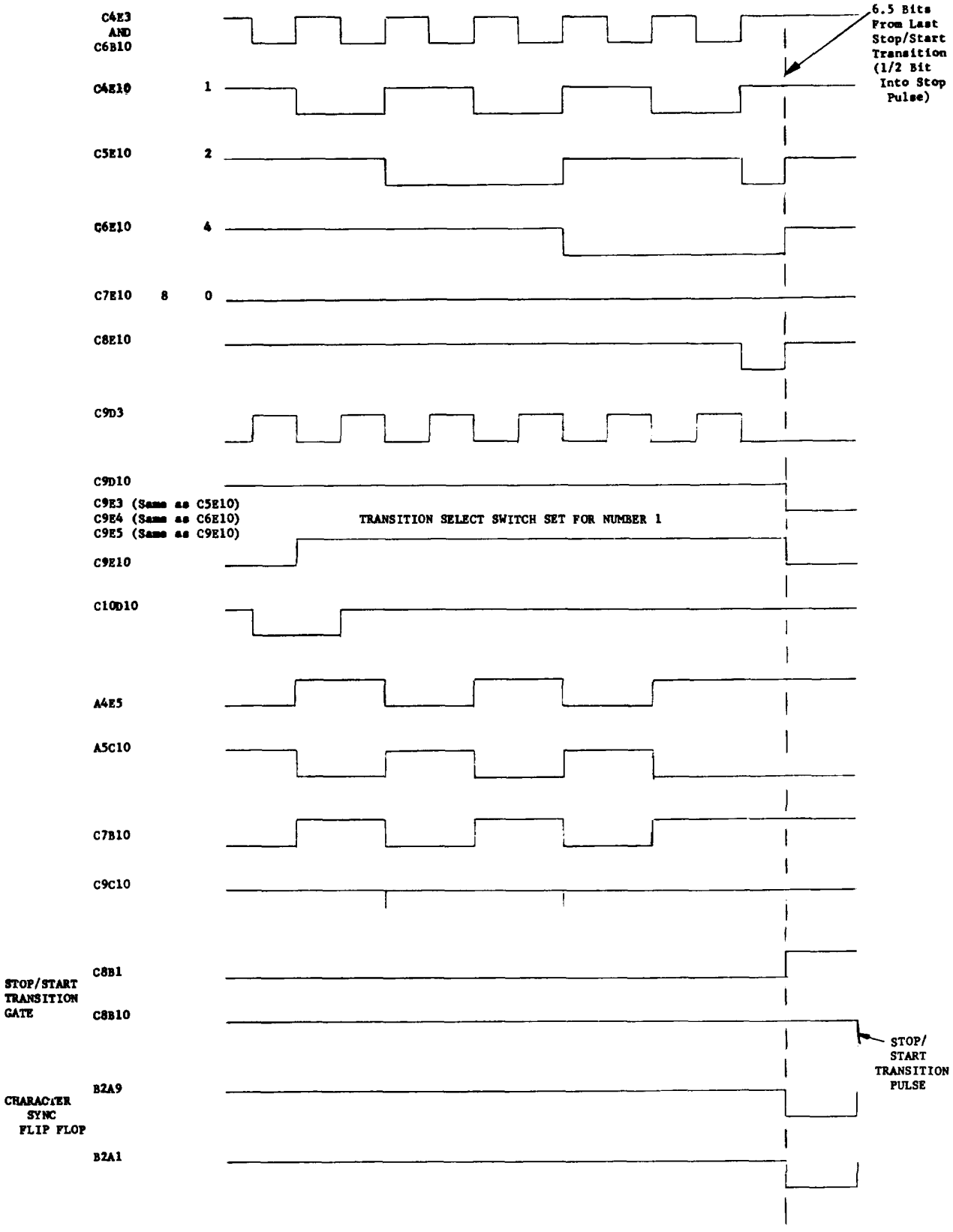


Figure 4-3. Data Analyzer, Waveforms (Sheet 3)

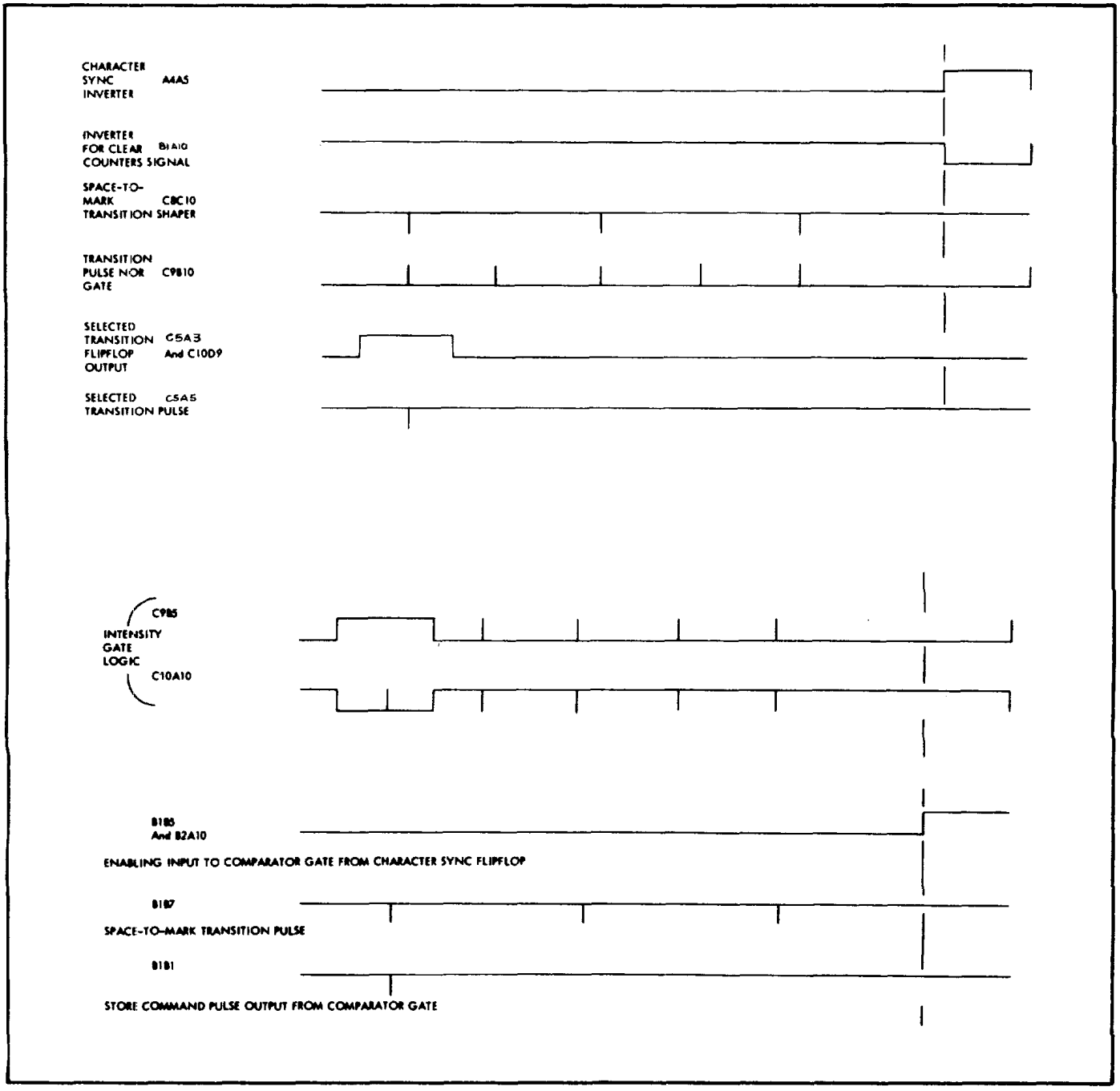


Figure 4-3. Data Analyzer, Waveforms (Sheet 4)

The count, contained in this up/down counter at the time of the input wave-form transition, constitutes the binary equivalent of the percent distortion. If the counter is counting up at the time of this transition, the transition occurred late. Conversely, if the counter is counting down at the time of input waveform transition this transition occurred early.

The operator may elect to read average distortion, total peak-distortion, early peak-distortion, or late peak-distortion by setting the DISTORTION SELECT switch to the appropriate position. The MARK to SPACE or SPACE to MARK toggle-switch in the TRANSITION SELECT switch area permits the operator to select either of these two types of transitions. If the operator sets the switch to the MARK to SPACE or SPACE to MARK position, as shown in block diagram 4-1, and sets the DISTORTION SELECT switch in the AVERAGE position, the comparator gate issues a store command to the storage register at each space-to-mark transition.

The digital comparator continuously compares the parallel content of the up/down counter to the parallel content of the storage register, and produces a negative-true output when the content of the up/down counter is greater than the content of the storage register. In the TOTAL PEAK position of the DISTOR TION SELECT switch the digital comparator output is ANDed with the mark-to space, or space-to-mark transition pulse and (in addition) with the "zero"-side output of the up/down control flip-flop, which results in a storage command to the storage register. In the LATE PEAK position of the DISTORTION SELECT switch, the digital comparator output is ANDed with the mark-to-space or space-to-mark

transition pulse and the "one" side of the up/down control flip-flop which results in a storage command to the storage register.

The digital-to-analog converter (hereafter called D/A Converter) uses six DA-1 modules. These modules are connected together in a D/A converter ladder circuit. The six parallel inputs of digital control information to the D/A converter ladder continuously examine the output of the storage register. Output current to the PERCENT DISTORTION meter is a linear analog equivalent of the count contained in the storage register.

Two additional outputs from the storage register provide early/late indications. These outputs are used to drive NOR-L modules connected as lamp drivers and are shown in the block diagram as triangular symbols.

In any of the peak positions of the DISTORTION SELECT switch readings the PERCENT DISTORTION meter is constantly updated by the comparator gate action previously described. The reading, at any given instant, is equal to the highest value entered into the storage register up to that moment. To clear the storage register and permit new readings, a reset input is provided. The miniature toggle-switch in the lower left-hand corner of the distortion select section provides the input to the reset bus. The switch is a spring-loaded type which returns from the DOWN position to CENTER and in the upper position has a stable RESET position. When the operator presses this switch, from its center position downward, a clear input is supplies to the storage register bank until the operator releases this switch to its center position.

In the upper position of this switch, the reset oscillator provides a reset pulse to clear the storage register at approximately 4-1/2 seconds intervals.

The input section provides for analysis of the following types of data telegraph signals:

(1) Low-impedance-polar with input sampling point near zero; that is, a change, from plus 2 ma through zero to -2 ma, is sensed as a mark-to-space, or space-to-mark transition according to the POLARITY switch setting.

(2) Twenty milliamperes neutral with a sampling point at approximately 10 ma, with operating differential in the 2 to 4 ma range.

(3) Sixty milliamperes neutral with sampling point near 30 ma; that is, in the 28 to 32 ma range.

(4) High-voltage, high-impedance polar intended for use on ground referenced 130 volts polar signal.

(5) Medium-voltage, high-impedance polar intended for ground reference polar signals in the 48 volts range.

(6) Low-voltage, high-impedance polar intended for use with signals in the 5 to 20 volts polar range.

Labeling of the input jacks on the front panel, and of the terminals at the rear panel, corresponds to the markings of the INPUT SELECT switch. Markings of the POLARITY switch indicate in which sense the Analyzer accepts the input signal; that is, plus indicates that the Analyzer accepts input signals of a positive marking sense at the tip of the input jack, either high impedance or low impedance and minus the reverse sense. The input light is provided to give a visual

indication of the input signal; that is steady "on" for steady mark, and steady "off' for steady space, and flashing for traffic. The FILTER IN OUT switch permits the operator to apply filtering to the input signal at low speeds on extremely noisy lines. At low modulation rates (that is below 150 baud) this filter does not introduce appreciable distortion. However, at the higher modulation rates, this filter should not be used.

Input shaping is provided by three CSR-M1 modules. These modules accept input mark-to-space or space-to-mark transitions, and release a negative-true pulse upon receipt of an input mark-to-space or space-to-mark transition from the input section.

The character-length counter is a four-stage binary ripple-through counter using four CSR-M1 modules. For start/stop telegraphy the operator sets the UNITS INTERVALS switch to the appropriate number of units in the code to be analyzed. This switch programs the outputs of the counter to the four inputs of a NOR-M module which, in turn, decodes a pulse related to the selected units interval. This pulse is logically combined with inputs from the up/down counter and the input shaping section to generate the following control signals for the Analyzer:

(1) A clear input to the four stages of the character-length counter;

(2) Character sync signal for the A-Scan;

(3) Blanking input to the A-Scan; and

(4) An input to the comparator gate to enable the comparator gate during the period of a character and disable it at the time of the STOP/START TRANSITION.

The TRANSITION SELECT switch programs the output of the character length counter stages to the four inputs of a medium-speed NOR-gate to provide a transition sync pulse to the A-Scan and to enable the comparator gate during the selected transition. This selected transition pulse starts 1/2-bit early to the transition selected for measurement, and ends 1/2-bit late.

The digital saw D/A converter, consisting of two D/A converter ladders, using D/A-1 modules, provides a negative-going ramp function for horizontal deflection of the A-Scan. This negative saw, or ramp function, is used to deflect the A-Scan when the SWEEP OPTIONS switch of the A-Scan is in the AUTO position.
The start of this saw is at the stop/start transition with fly-back occurring when the character-length counter is cleared.

The intensity marker generator, consisting of two Dual-NOR gates, logically combines the mark-to-space transition pulse, the space-to-mark transition pulse, and the 1-bit-wide selected transition gate from the character-length generator to produce intensity markers for the A-Scan.

4-2. DETAILED PRINCIPLES OF OPERATION

4-3. CLOCK DIVIDER (See Logic Diagram, Figure 4-2)

The input stage of the clock divider is a CSR-M module connected as a buffer inverter. This inverter supplies a 3.84-mc clock signal to the trigger input of the first flip-flop in the clock-divider chain. Baud rates of 37.5, 75, 150, 300, 600, 1209, 2400, 4800 and 9600 are tapped directly by the BAUD RATE switch shown in the logic diagram. The programmed pre-setting system, used in this clock-divider chain, permits generation of over 1000 additional non-integer baud rates. Baud rates that are not binary functions of 3.84-mc are provided by programmed presetting of the clock-divider chain.

4-4. PROGRAMMING COUNTER CHAIN FOR BAUD RATES

Assuming the first flip-flop (located in module position B2E) has a binary weight of 2^0, then the following stages appear as 2^1 through 2^9. A binary weight of 2^0 on the first flip-flop permits the use of a 3.84-mc timing source. To obtain a frequency from the clock divider of 5560-cycles-per second (100 x 55.6 baud) a flip-flop output must be selected which has a slower counting rate, and numbers are then injected into the counter to increase the speed. For 5560 cycles/sec the output is obtained from the 2^9 stage (normally 3750 cycles/sec).

If the timing source (3.84-mc) is divided by 5560 and rounded off, the nearest whole number will be 691.

The full count of the clock divider chain is 1024.

For example:

1024 - 691 = 333

333 = 256 + 64 + 8 + 4 + 1

Therefore, for an output of 5560 cycles/sec, the 256, 64, 8, 4 and 1 flip-flops must be set at the beginning of each cycle.

This presetting is done via the BAUD RATE switch and patch jumpers located in module locations D3E through D10E. A CSR-M1 module, in location C3E, produces a pulse of approximately 140 nanoseconds to accomplish this presetting. The 1/2 Dual-NOR module (in location C2E), wired as a power driver, provides the pulse amplitude required to preset the number of flip-flops involved.

The waveforms shown for the clock-divider sections are made at 4800 baud. The waveforms at flip-flop C1E become non-symmetrical for modulation rates below 75 baud, with the exception of 37. 5 baud.

4-5. UP/DOWN COUNTER

The up/down counter proper consists of six CSR-Ml modules, arranged with NOR-gating in a reversible binary parallel-clocked counter configuration. Up/down control is provided by the CSR-Ml module in location D4C.

This flip-flop provides up and down control with a negative pulse, on pin 10, equivalent to an up count. This signal is wired to B9A3, B10A3, B9B3, B10B3 and B9C3 to inhibit these NOR-gates during the up count. Thus, the carry from stage-to-stage is taken from the "one" side of each flip-flop when counting up. During the down count this signal is "zero. " The output from pin 9 of D4C is wired to B3B3, B4 B3, B5B3, B6B3 and B7B3, to inhibit these NOR-gates. Thus the carry from stage-to-stage is taken from the "zero" side of each flip-flop when counting down.

DG-1 module, in location D2C, and 1/2 Dual-NOR module, in D3C are used to decode a count of "zero" and set the control flip-flop to the "one" or up condition. DG-1 module, in location D1C, and the other half of Dual NOR module, in location D3C, are used to decode a count of 50 and to clear the up/down control flip-flop for 50 turn-around. CSR-ML module, in location C4E, provides one trigger pulse to the character-length counter per cycle of the up/down counter.

4-6. DIGITAL FULL COMPARATOR

The digital comparator operates on a bit-by-bit basis as it continuously compares the parallel content of the up/down counter to the parallel content of the storage register. The gating involved with the most significant bit, (that is, 32 in the counter and storage register) has three possible outputs.

This same principle is carried on throughout the comparator. These out puts are as follows: If counter 32 flip-flop (B8A) is in the "one" state (B8A10 negative) and storage 32 flip-flop is in the "zero" state (B8C10 at ground) the level at B8B10 will be negative; the comparator output will be negative, and the comparison is complete. This condition exists when the number in the counter contains a 32; that is, a number 32 or larger and the number stored is less than 32. In the event the counter 32 flip-flop and the storage 32 flip-flop are both equal; that is, both at ground potential (both containing "zero's") or both negative (both containing "one's) the output of B8B10 will be "zero, " the output of C5A10 will be "zero," and the comparison of the next less-significant bit will be enabled because the two inputs to the two-input OR-gate are at ground. If storage flip-flop B8C (output pin 10) is negative, and counter 32 flip-flop B8A is in the "zero" state (B8A10 at ground) the output of NOR-gate C5A (pin 10) will be negative. This negative output is connected as an input to the remaining OR-gates to inhibit any further comparison of less significant bits.

In the event of equal indications from the most-significant bit comparison, the input to B7B1 and C4A3 is "zero," thus enabling these NOR gates to perform comparison of the 16 counter and 16 storage bits.

When the DISTORTION SELECT switch is any of the PEAK positions, an output from the 1/2 Dual-NOR (B10D10) is provided as an input to AND-gate. This same principle is carried on throughout the comparator. These outputs are as follows: if counter 32 flip-flop (B8A) is in the "one" state (B8A10 negative) and storage 32 flip-flop is in the "zero" state (B8C10 at ground) the level at B8B10 will be negative; the comparator output will be negative, and the comparison is complete.

This condition exists when the number in the counter contains a 32; that is, a number 32 or larger and the number stored is less than 32. In the event the counter 32 flip-flop and the storage 32 flip-flop are both equal; that is, both at ground potential (both containing "zero's") or both negative (both containing "one's") the output of B8B10 will be "zero", the output of C5A10 will be "zero", and the comparison of the next less-significant bit will be enabled because the two inputs to the two-input OR-gate are at ground. If storage flip-flop B8C (output pin 10) is negative, and counter 32 flip-flop B8A is in the "zero" state (B8A10 at ground) the output of NOR-gate C5A (pin 10) will be negative. This negative output is connected as an input to the remaining OR-gate to inhibit any further comparison of less significant bits.

In the event of equal indications from the most-significant bit comparison, the input to B7B1 and C4A3 is "zero", thus enabling these NOR-gates to perform comparison of the 16 counter and 16 storage bits.

When the DISTORTION SELECT switch is any of the PEAK positions, an output from the 1/2 Dual-NOR (B10D10)

is provided as an input to AND-gate B1B (pin 10). The signal enables transfer into storage only when the digital comparator output is negative indicating a number in the counter rather than the number in storage.

4-7. STORAGE REGISTER

The storage register consists of seven CSR-M1 flip-flops with trigger inputs bussed together and steer inputs connected for parallel transfer from the up/down counter. The seventh flip-flop stores the condition of the up/down control system at the time of the input transition involved in the measurement. This flip flop is in location B2C and is designated Early/Late on the logic diagram. When it contains a "one", the early light is lighted and, conversely, when it contains a "zero" the late light is lighted.

4-8. COMPARATOR GATE

The comparator gate is a type DG-1 module in location B1B. This module is wired as five-input AND-gate. Mark-to-space or space-to-mark transition pulses are ANDed with other signals by the setting of the DISTORTION SELECT switch as follows:

Average (AVG) - With enabling gate from character-length counter B2A10, and with selected transition pulse from character-length counter C10D10.

TOTAL PEAK - With the two inputs above (B2A10, C10D10), and with the digital comparator output from B10D10.

EARLY PEAK - With the three inputs above (B2A10, C10B10, B10D10), and with the "zero" side output of the up/down control flip-flop D4C.

LATE PEAK - With the three inputs (B2A10, C10D10, B10D10) and with the "one'-side output of the up/down control (D4C).

4-9. DIGITAL-TO-ANALOG CONVERTER AND METER-DRIVE CIRCUITRY

The function of the D/A converter module is described in detail in figure 5-7. The source impedance of the D/A converter ladder is 2000 ohms. With the PERCENT DISTORTION meter properly calibrated the output voltage of the D/A converter, at pin B8D5 (as measured with a high-impedance digital volt meter)) should be 3.889 volts for 49% distortion.

Provision is made at the rear-panel terminals for the addition of one or more external meters. As shipped, the Analyzer has a jumper provided between the minus (-) external meter and the plus (+) external meter rear terminals to permit normal operation with internal meter only. A single external meter, of the type used on the front panel, may be connected between the minus (-) external meter terminals and plus (+) external meter and signal ground terminals. This provides a short across the 100 ohms resistor, normally provided between plus (+) external meter terminal and signal ground terminal; and the 100 ohms extra impedance of the external meter will now leave the calibration unchanged. If more than one external meter is desired, these may be connected in series, and the meter calibration trimpot, mounted on the rear of the front panel meter is readjusted for 49% readout with 49% distortion.

4-10. INPUT SECTION - LOW IMPEDANCE OPERATION

The impedance, looking into the low-Z jack, is 100 ohms. This resistance is the series-parallel equivalent value of two 100 ohms 1/2 watt resistors in parallel (wire-wrapped between pins A3E7 and A1E7) and of two 100 ohms 1/2-watt resistors in parallel in the threshold detector modules. The simplified low-Z input loop circuits (figure 4-4) illustrates the path taken by the input current as it passes through the input section.

CAUTION

When applying a signal in low-Z input condition, the input current should not exceed 100 ma.

NOTE
The input impedance is 100 ohms, there fore the input voltage should not exceed 10 volts.

Low-impedance sampling input points are factory preset as follows: Input adjustment R7 is preset to sample at "zero" for low-impedance polar. Input adjustment R6 is preset to sample at 10 ma for 20-ma neutral. Input adjustment R5 is preset to sample at 30 ma for 60-ma neutral.

Referring to the logic diagram (figure 4-2) the 30 megacycle oscillator No. 2, in module location A3D and A4D, is switched ON and OFF by the threshold detector in module location A3E. This switching occurs at the instant the input

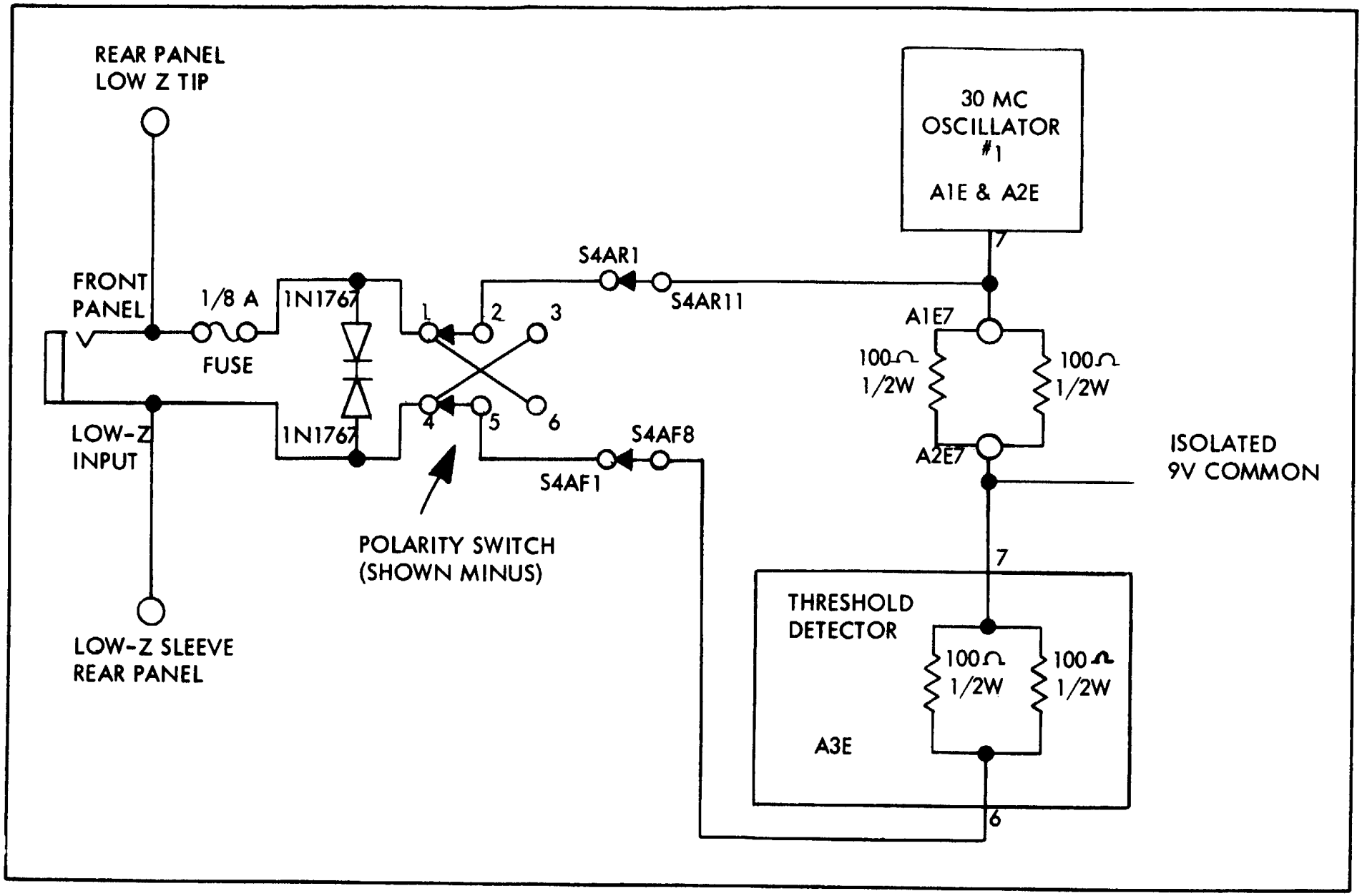


Figure 4-4. Simplified Low-Z Input Loop Circuit

current value crosses the threshold preset into the threshold detector module. The 30-megacycle oscillator provides DC-isolation from input to output circuits which are operated at signal ground reference levels. The output switch module, in location A4E, filters the output of the 30-megacycle oscillator No. 2, and converts this level to normal DC logic levels required by the dual-NOR module in location A5C.

The 30-megacycle oscillator No. 1, in location A1E and A2E, provides DC-isolation for the oscilloscope input. The DC output of this module bears a linear relationship to the low-Z input current. The A-scan output module, in location A1D and A2D, filters and buffers this output signal.

4-11. INPUT SECTION - HIGH IMPEDANCE OPERATION

The simplified high-Z circuit diagram (figure 4-5) illustrates the variation when the Analyzer is used with high-Z input. The primary difference is that the high Z input module, in location A5D and A6D is inserted ahead of the low-Z input loop shown in figure 4-4.

NOTE

The high-Z input is signal ground referenced rather than ground isolated as in the case of the low-Z input.

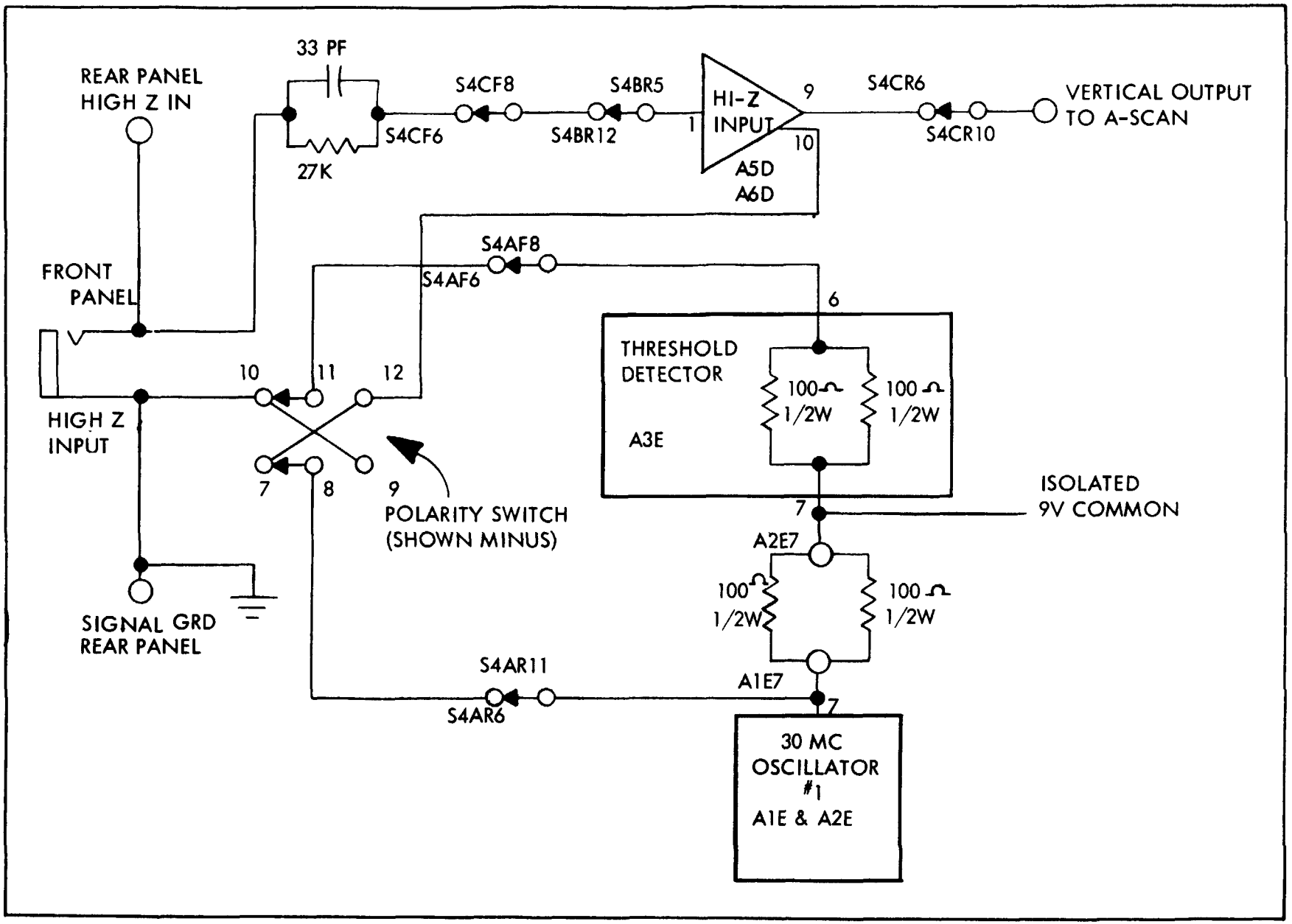


Figure 4-5. Simplified High-Z Input Circuit Diagram

4-12. CHARACTER-LENGTH COUNTER

The action of the character-length counter bears a close relationship to the electro-mechanical action of a telegraph distributor. When the output of flip-flop B2A (pin 9) is negative, the up/down counter and the character-length counter are held in a cleared condition analogous to the stationary locked position of the telegraph distributor. In both cases the next mark-to-space transition is interpreted as the Stop-to-Start transition, and the timing of the new character has begun.

Assuming that the input is resting in steady mark, the truth-table (Table 4-1) indicates the state of the various gates and flip-flops as a character is entered into the instrument. The first line of this truth table titled, "Last Part of Stop Pulse, or, Resting in Steady Mark" indicates the logical beginning of the character-length counter operations. The diagram of the simplified character length counter proper (figure 4-6) is referenced in the following discussion of the character length counter operation.

When resting in steady mark during the last part of the stop pulse, gate C8B (dual-NOR) is enabled for a mark-to-space transition pulse. This condition is brought about by flip-flop B2A resting in the cleared condition. At the leading edge of the mark-to-space transition pulse the output of gate C8B (pin 10) goes negative, and at the trailing edge this level returns to ground. This positive-going transition of the trailing edge of the mark-to-space transition pulse serves as a

Table 4-1. Character length Counter Truth Table.

Logic 1 Level = -4.42 to -10 VDC Logic 0 Level = +0.5 to -0.2 VDC	Character Sync FF B2A9	Character Sync FF B2A10	UP/DN Control FF C4B10	1 FF C4E10	2 FF C5E10	4 FF C6E10	8 FF C7E10	Number in Character Length Counter	Units Interval Decoder NOR C8E10	Units Interval FF C9D10	Transition Select Gate NOR C9E10	Selected Transition FF C10D10
			1=UP									
Last Part of Stop Pulse, or, Resting in Steady Mark	1	0	1	0	0	0	0	0	0	1	1	0
1/4 BIT Following Stop/Start Transition	0	1	1	0	0	0	0	0	0	0	1	0
3/4 " " " " "	0	1	0	0	0	0	0	0	0	0	1	1
1 1/4 " " " " "	0	1	1	1	0	0	0	1	0	0	0	1
1 3/4 " " " " "	0	1	0	1	0	0	0	1	0	0	0	0
2 1/4 " " " " "	0	1	1	0	1	0	0	2	0	0	0	0
2 3/4 " " " " "	0	1	0	0	1	0	0	2	0	0	0	0
3 1/4 " " " " "	0	1	1	1	1	0	0	3	0	0	0	0
3 3/4 " " " " "	0	1	0	1	1	0	0	3	0	0	0	0
4 1/4 " " " " "	0	1	1	0	0	1	0	4	0	0	0	0
4 3/4 " " " " "	0	1	0	0	0	1	0	4	0	0	0	0
5 1/4 " " " " "	0	1	1	1	0	1	0	5	0	0	0	0
5 3/4 " " " " "	0	1	0	1	0	1	0	5	0	0	0	0
6 1/4 " " " " "	0	1	1	0	1	1	0	6	1	0	0	0
6 3/4 BIT Following Stop/Start Transition	1	0	1	0	0	0	0	0	0	1	1	0

NOTE: The conditions at 6 3/4 are identical to the first line hence the completion of one character. Transition select decoder gate waveform and table entries are with transition select switch set for one.

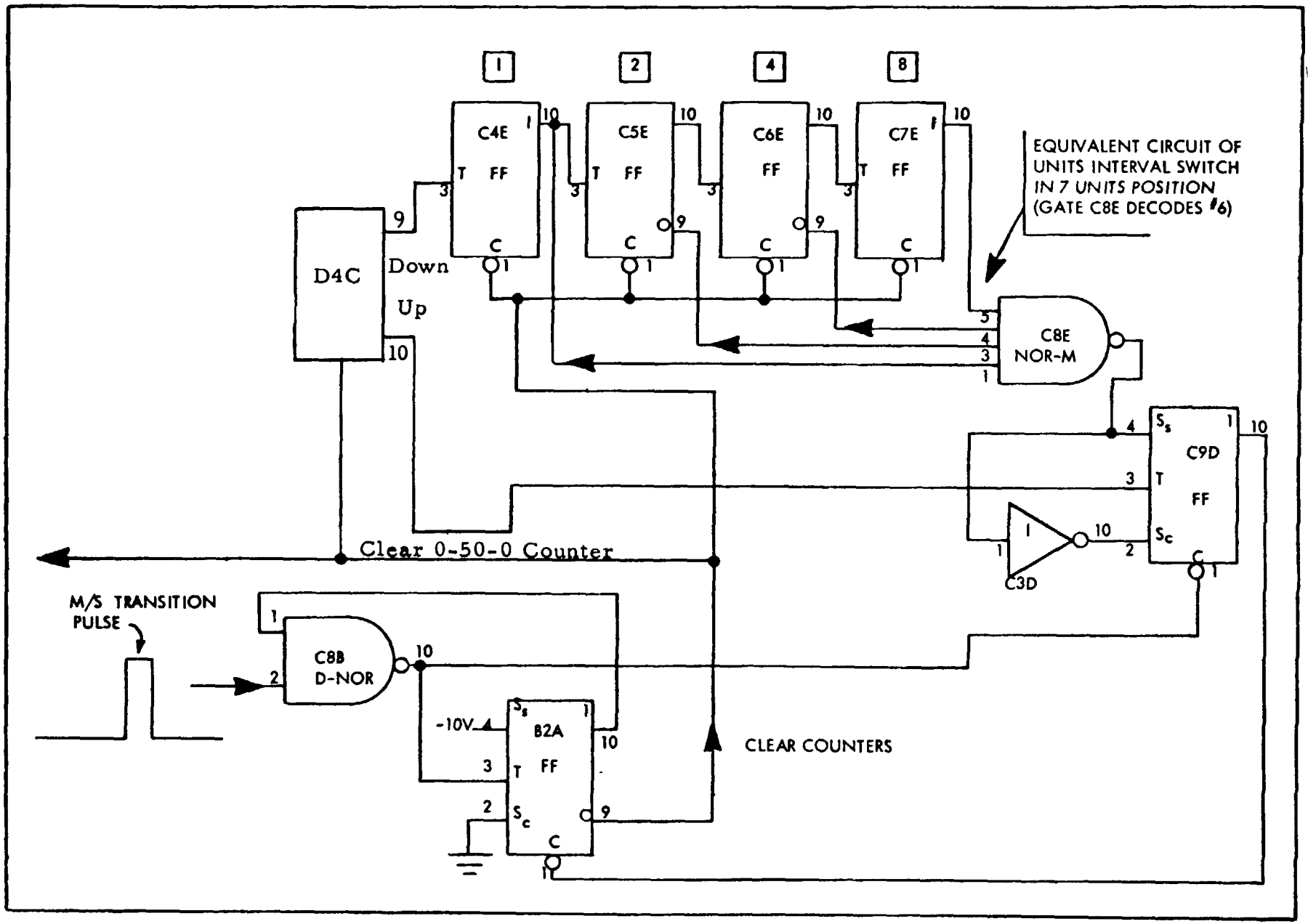


Figure 4-6. Simplified Character-Length Counter

trigger input to flip-flop B2A which then goes from "zero" to "one" state because steering input (pin 2) steer clear is at ground, and steering input (pin 4) steer is set at minus 10 volts. When the output of C8B10 went negative at the leading-edge of the mark-to-space transition pulse, this output was also used to clear flip-flop C9D preparatory to the next Stop pulse of the incoming character.

The simplified character-length counter diagram (figure 4-6) shows up-down flip-flop D4C as a reference for the source of two signals used in the character-length counter operation. For the purposes of this discussion the equipment is assumed to be set for Baudot Code selected character "Y," the transmitter sending a 7.42 unit code and the Analyzer UNIT INTERVALS switch set for 7 units.

The character-length counter is advanced one count for each bit of the incoming code at the end of that bit; that is, it is advanced one count at the end of the Start pulse, one at the end of the first pulse, one at the end of the second pulse, one at the end of the third pulse, one at the end of the fourth pulse, and one at the end of the fifth pulse which is at the beginning of the Stop pulse.

Therefore, at the beginning of the Stop pulse, the counter has been advanced to the count of six, and so for seven units code the inputs to the NOR-M module C8E are programmed to decode the sixth pulse as indicated on the simplified diagram. Furthermore, for each selected units interval position, gate C8E decodes a number from the character-length counter which is one indicated on the front panel. At 6.5 bits from the start/stop transition (1/2 bit into the stop pulse) the

positive-going edge of the waveform of the up-down flip-flop (D4C, pin 10) triggers flip-flop C9D to the set or "one" condition. This "one" output of flip-flop C9D (pin 10) serves as a clear input to flip-flop B2A (pin 1) completing the cycle, resetting the character length counter to "zero" condition via its clear bus to pin 1 of flip-flops C4E, C5E, C6E and C7E, and simultaneously enables C8B (NOR-gate) to pass another mark-to-space transition pulse which should be the Stop/Start transition of the next character.

To insure that the up/down counter is also at "zero" at the beginning of the next character, pin 9 (the "zero" output of flip-flop B2A) is connected to the clear inputs of the up/down counter via the START/STOP SYNCHRO NOUS switch.

SECTION V

LOGIC MODULES

(Operation and Application Notes)

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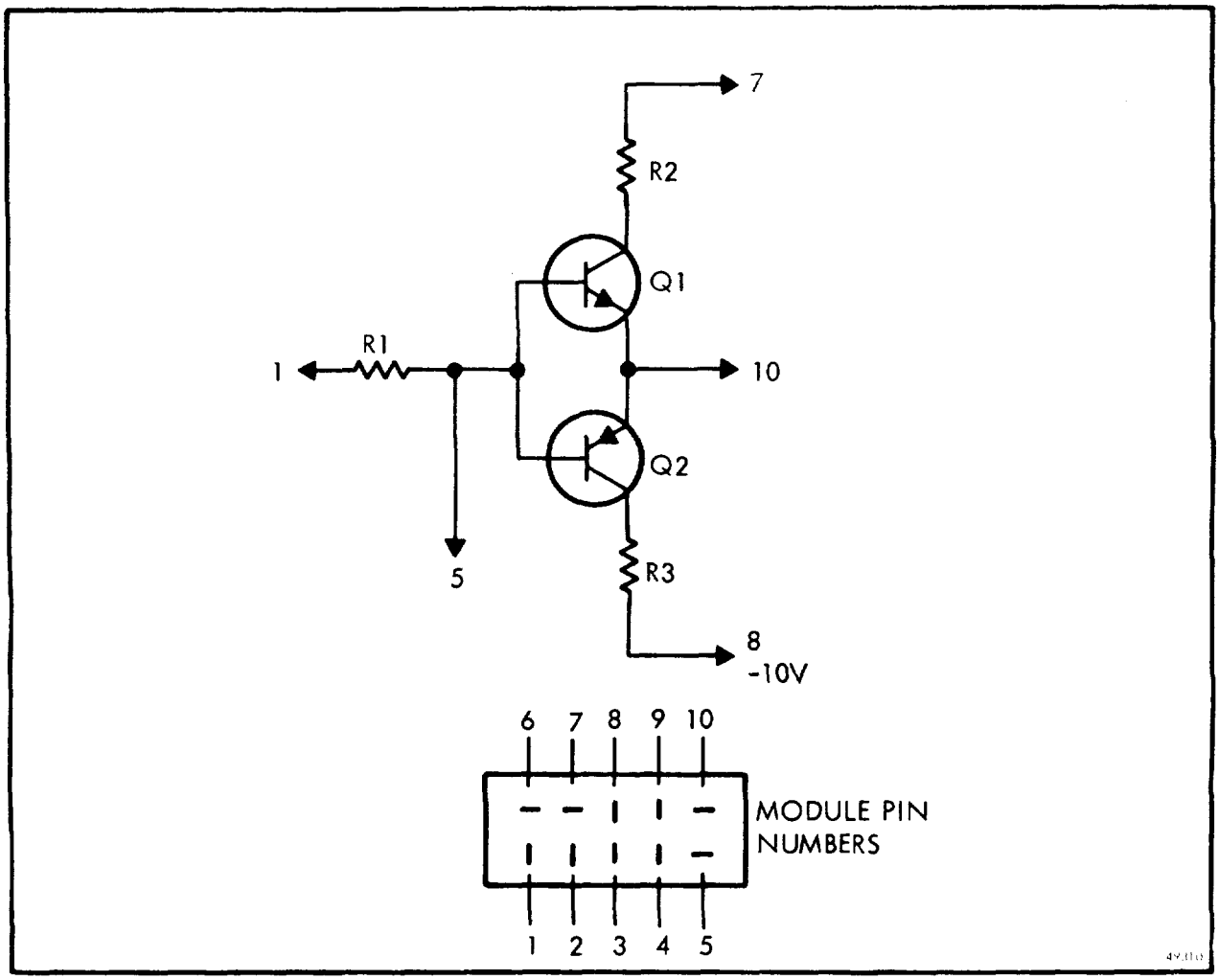
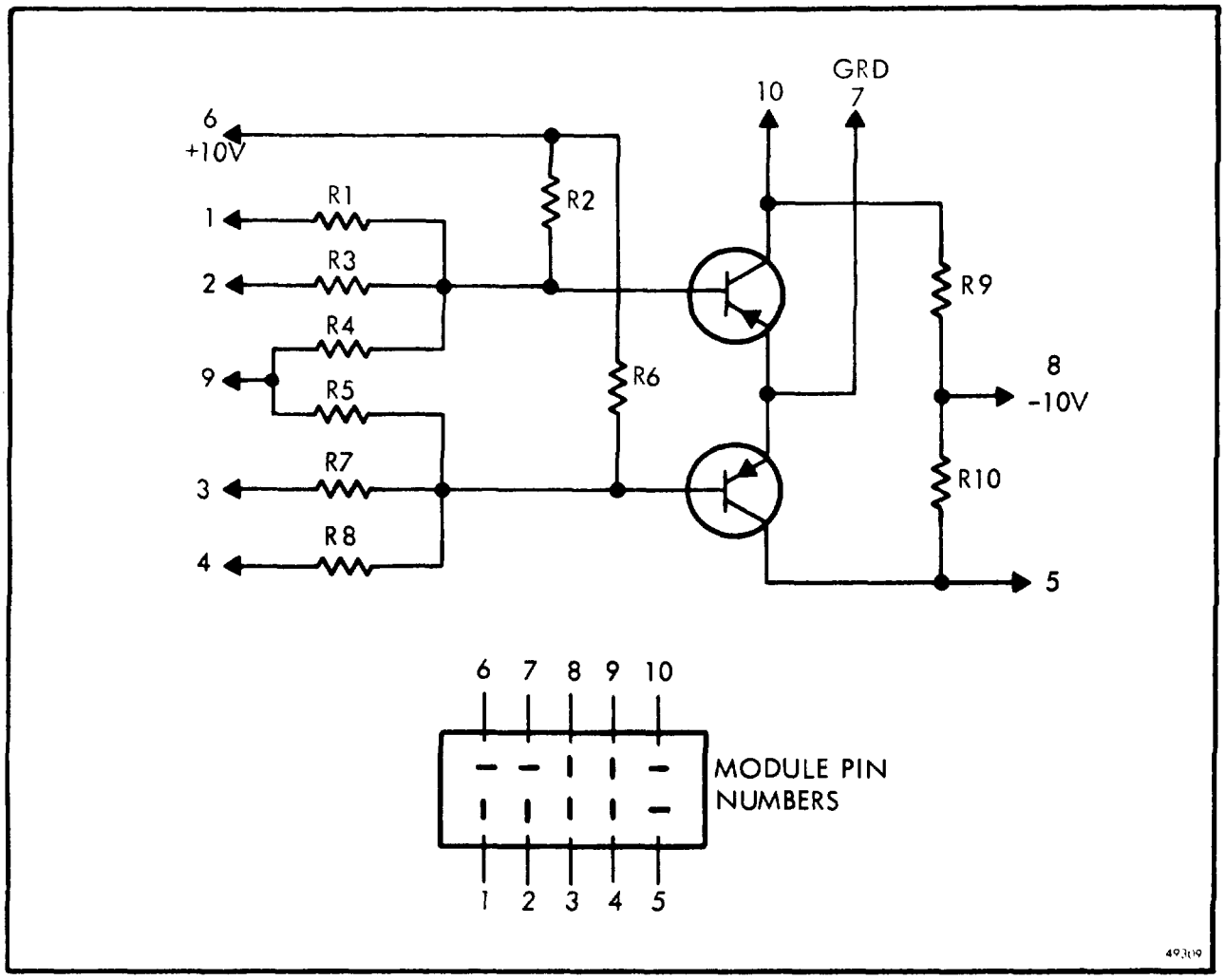


Figure 5-1. Buffer Amplifier (Module 506065G2)

The circuit is a complementary emitter-follower and is used, when needed, to provide larger fan-out capability.

The input resistor (R1) isolates the driving circuit from any capactive loading on the output.

The Buffer Amplifier odds negligible delay to low or medium-speed input waveforms.

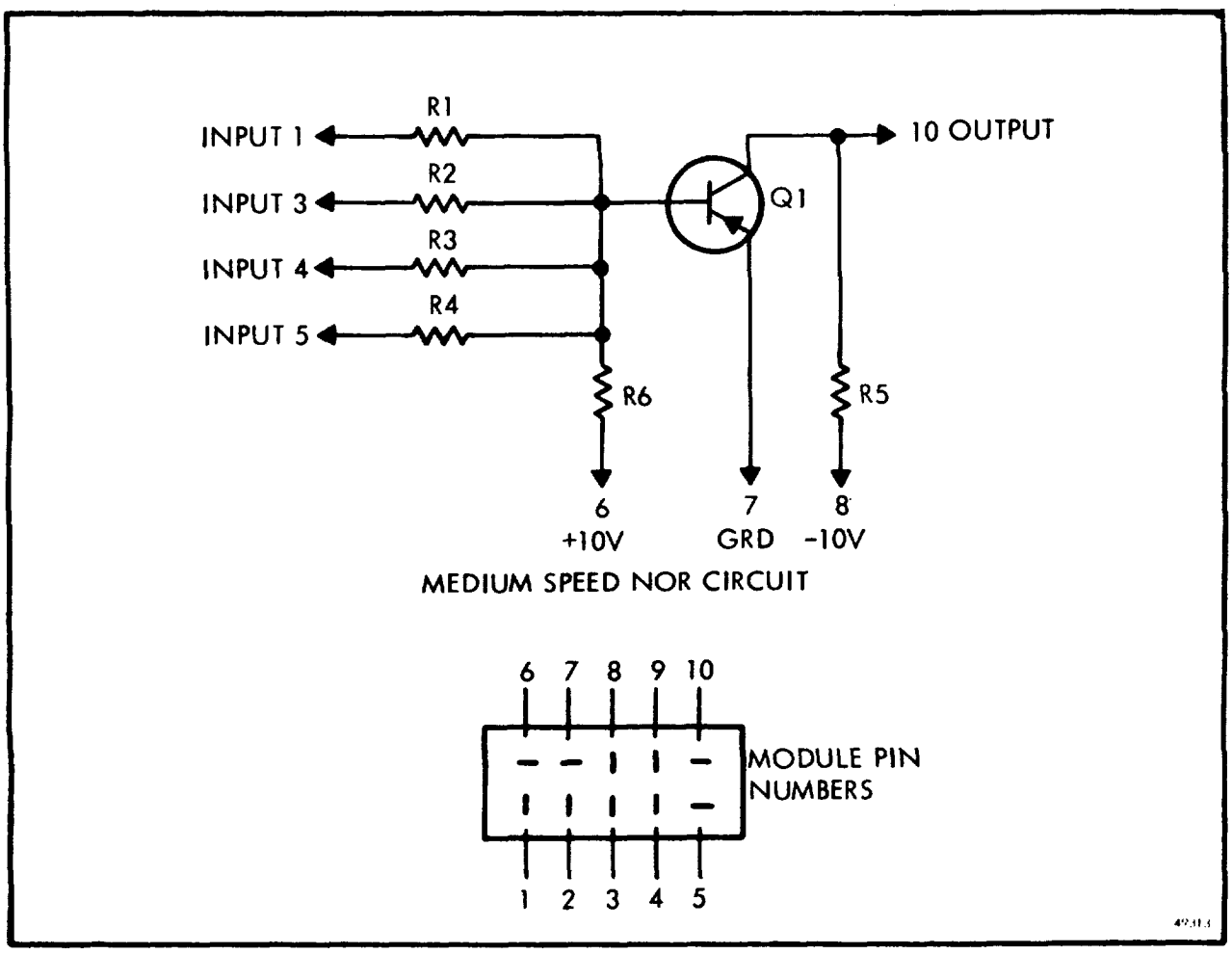


The Dual-NOR consists of two three-input logic NOR's within one module. Each NOR has separate inputs and one shared input.

The output at pin 10 will be 0.0 to -0.2 volts if inputs 1 or 2 or 9 are more negative than -5.7 volts. The output at pin 10 will be -5 to -10 volts (depending on the loading) if inputs 1, 2 and 9 are all more positive than -0.2 volts. (An open input has the same effect as a grounded input.)

The output at pin 5 will be 0.0 to -0.2 volts if input 3 or 4 or 9 is more negative than -5.7 volts. The output at pin 5 will be -5 to -10 volts if inputs 3, 4 and 9 are all more positive than -0.2 volts.

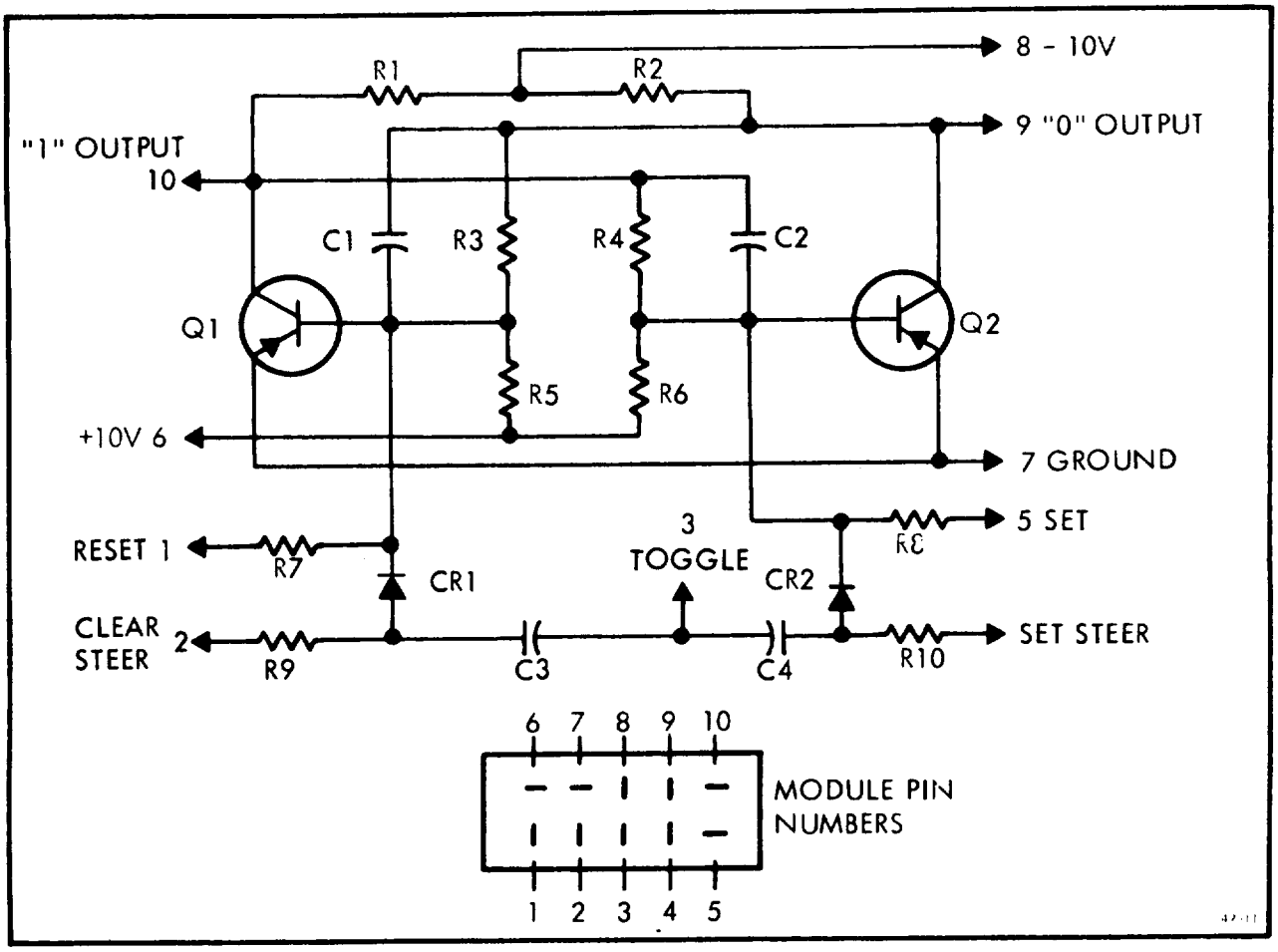
Figure 5-2. Dual-NOR (Module 509033)



The operation of a NOR module is such that if one input is more negative than -5.65 volts and the other three inputs are at ground or any negative voltage level the transistor is saturated. Under these conditions the output voltage is between 0 and -0.2 volt. If all four inputs are connected to the outputs of saturated transistors, the gating transistor is turned off, producing a nominal unloaded output of -10 volts. Connection of the maximum loads can decrease the negative amplitude to approximately -5 volts.

The operation of the NOR gate enables the performance of both the logical AND and OR functions with a single circuit. It inverts the logic levels in both cases. For negative-true inputs (logic "one" corresponding to -5 volts), the circuit performs the OR-NOT function F= A+ B. For positive-true logic (logic "one" corresponding to 0 volt), the circuit performs the AND-NOT function F = AB. Therefore, all combination gating functions may be performed .with the NOR circuit by using positive-true logic to perform AND functions and negative true inputs to perform OR functions.

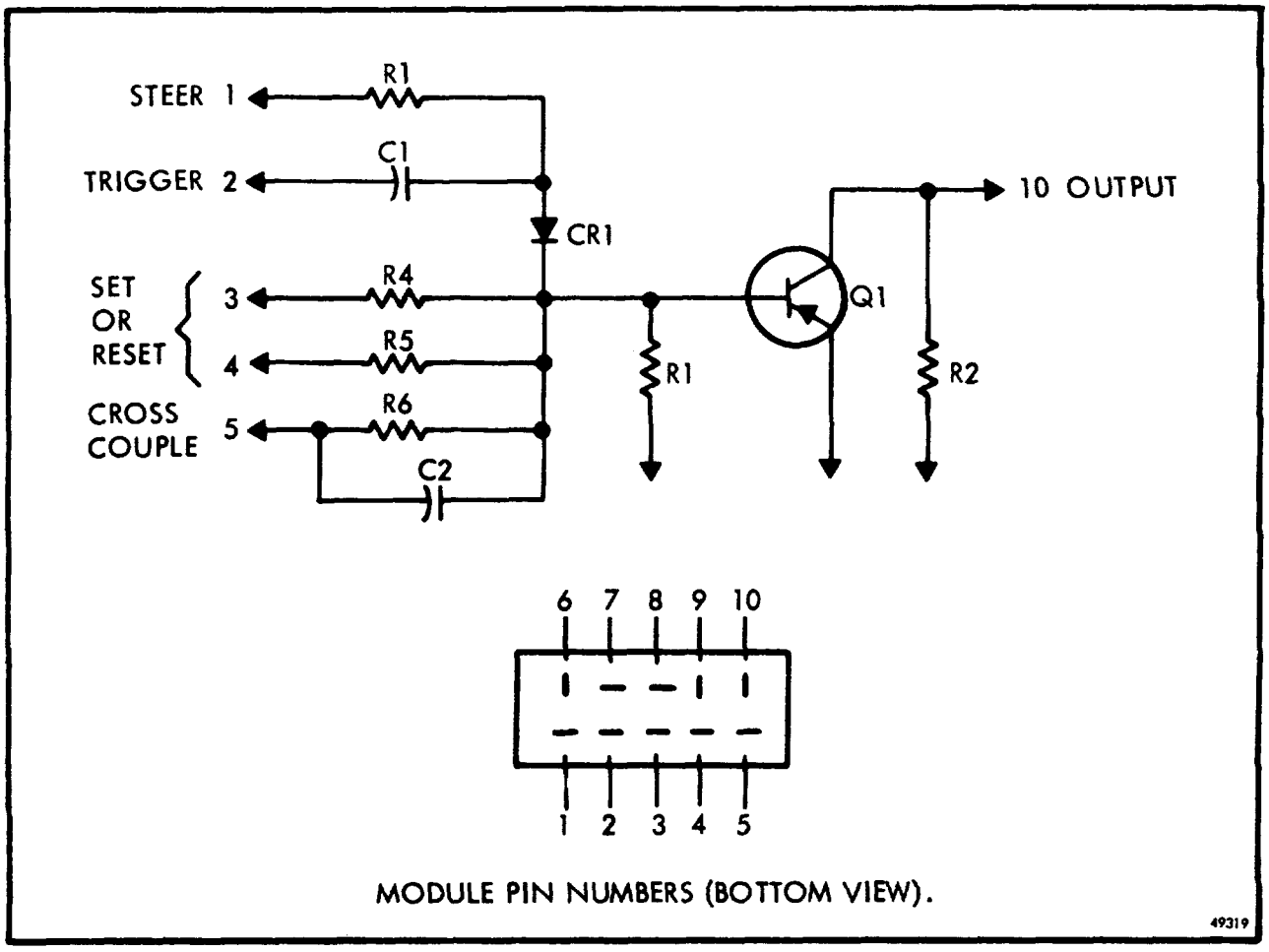
Figure 5-3. NOR-M Medium-Speed NOR (Module 503815)
(This is also NOR-L Configuration)



A single CSR module is required to form a complete counter shift register circuit. The circuit output levels may be switched by either the DC SET and CLEAR inputs or by the STEER and TRIGGER inputs.

Switching of the CSR occurs only when the trigger input makes a positive transition and the DC set and clear inputs are at ground voltage level. If one steer input is at ground voltage level and the other is more negative than -5 volts, the CSR circuit outputs assume the some logic levels that the corresponding inputs had at the time of switching, the "1," output being equal to the steer set (S_S) and the "0" output being equal to the steer clear (S_C) input. If both steer inputs are negative when the trigger input makes a positive transition, no switching occurs. If both steer input are at ground level when the trigger makes a positive transition, the operation of the circuit is undefined. Shift registers are formed by connecting "1" output of the CSR circuit to S_S input of the next stage and the "0" output to the S_C input of the next stage. Counters are formed by connecting the "1" output of each stage to the trigger input of the next stage. In each stage the "1" output is connected to the S_C input and the "0" output to the Ss input of the some stage. These connections are not shown on the logic diagrams in the interest of simplification.

Figure 5-4. CSR-M1 Medium-Speed Counter Shift Register (Module 506030)

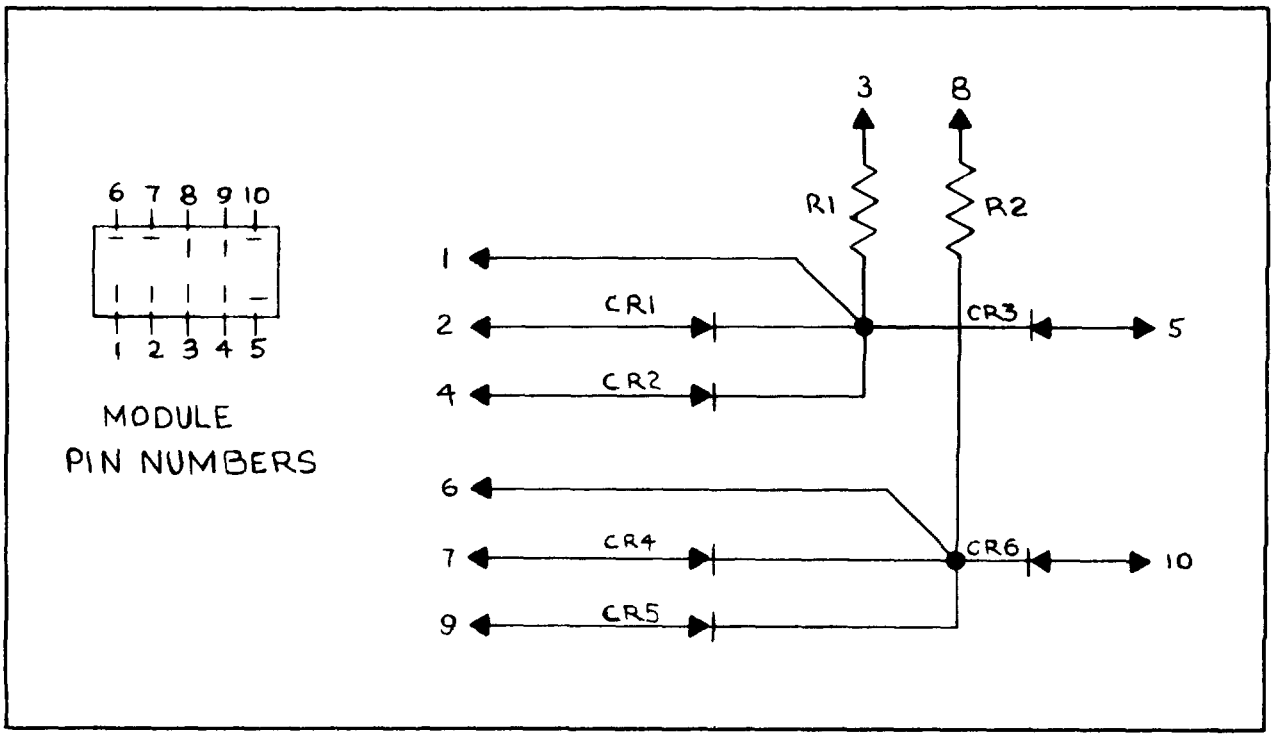


Two identical CSR-M modules are required to form a complete counter shift register circuit. The circuit output levels may be switched by either the d-c set and clear inputs or by the steer and trigger inputs.

The set or clear input must be made more negative than -5.03 volts to switch the CSR. However, if both inputs are made negative, both transistors are turned on for the duration of the negative input signals.

Switching of the CSR occurs only when the trigger input makes a positive transition and the d-c set and clear inputs are at ground voltage level. If one steer input is at ground voltage level and the other is more negative than -5 volts, the CSR circuit(2 CSR-M modules) outputs assume the same logic levels that the corresponding inputs had at the time of switching, the "1" output being equal to the steer set (S_S) and the "'0" output being equal to the steer clear (S_C) input. If both inputs ore negative when the trigger input makes a positive transition, no switching occurs. If both steer inputs are at ground level when the trigger makes a positive transition, the operation of the circuit is undefined.

Figure 5-5. CSR-M Counter Shift Register (Module 503819)

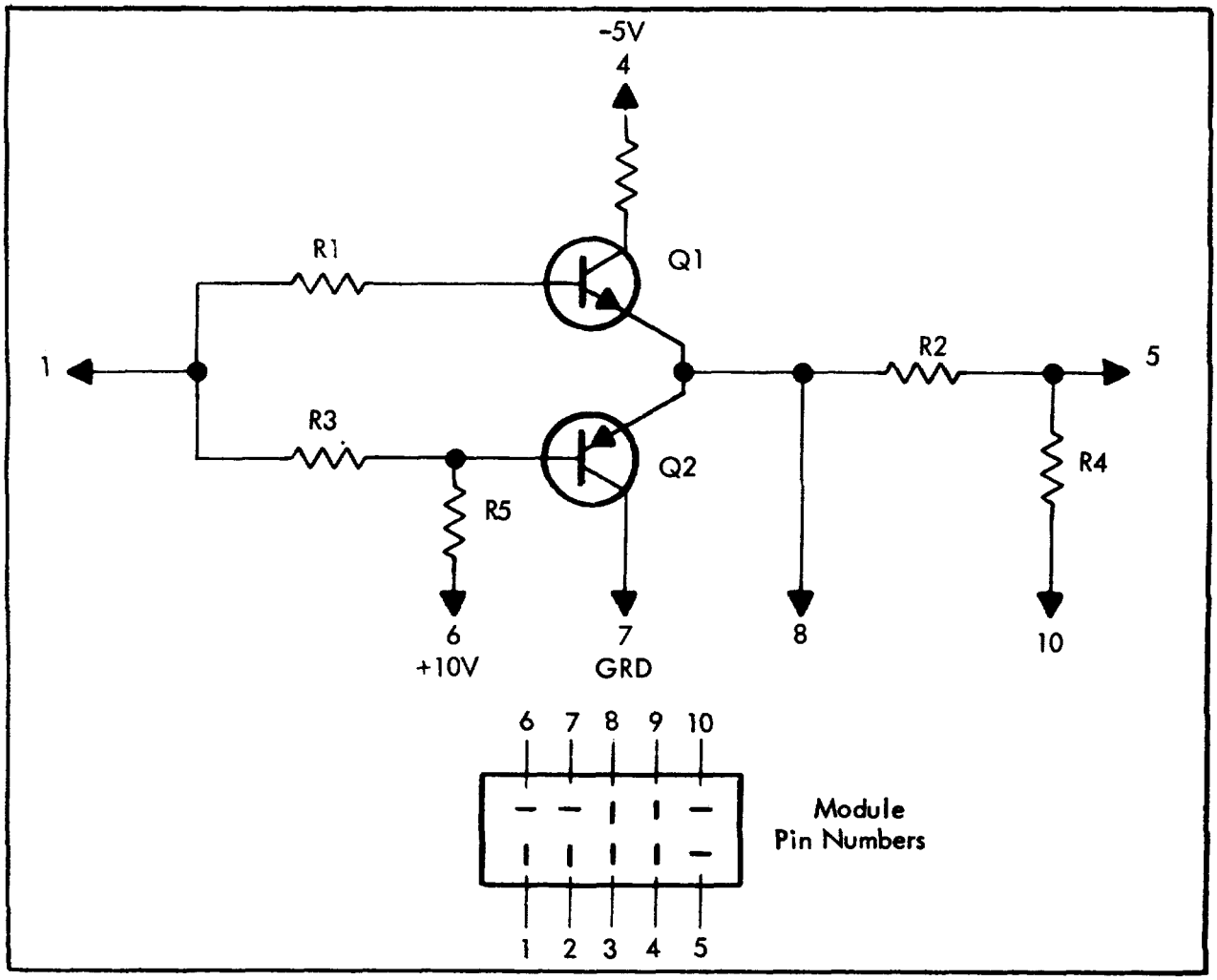


Two three-input negative coincidence diode gates are contained in one module when pins 3 and 8 are returned to -10 volts.

An exclusive OR may be formed using this module when pins 5 and 10 are externally tied together and biased with 8.2K ohm resistor to +10 volts (output at pins 5 and 10).

This module may be used with other standard modules but each application should be individually evaluated.

Figure 5-6. Diode Gate (Module 505694)



The D/A module is designed to operate as a driver for a binary or BCD voltage ladder. When the modules are wired in an 8-bit binary ladder configuration, the impedance in series with the voltage generator is 2K ohms.

The digital input control is typically single ended zero or -6.5 volts on pin 1. With an input of zero volts, transistor Q1 is conducting and the reference voltage (-5V) appears on pin 8. If the input is -6.5 volts transistor Q2 conducts and the voltage on pin 8 is zero volts.

Figure 5-7. Digital-to-Analog Converter (Module 505703G4)

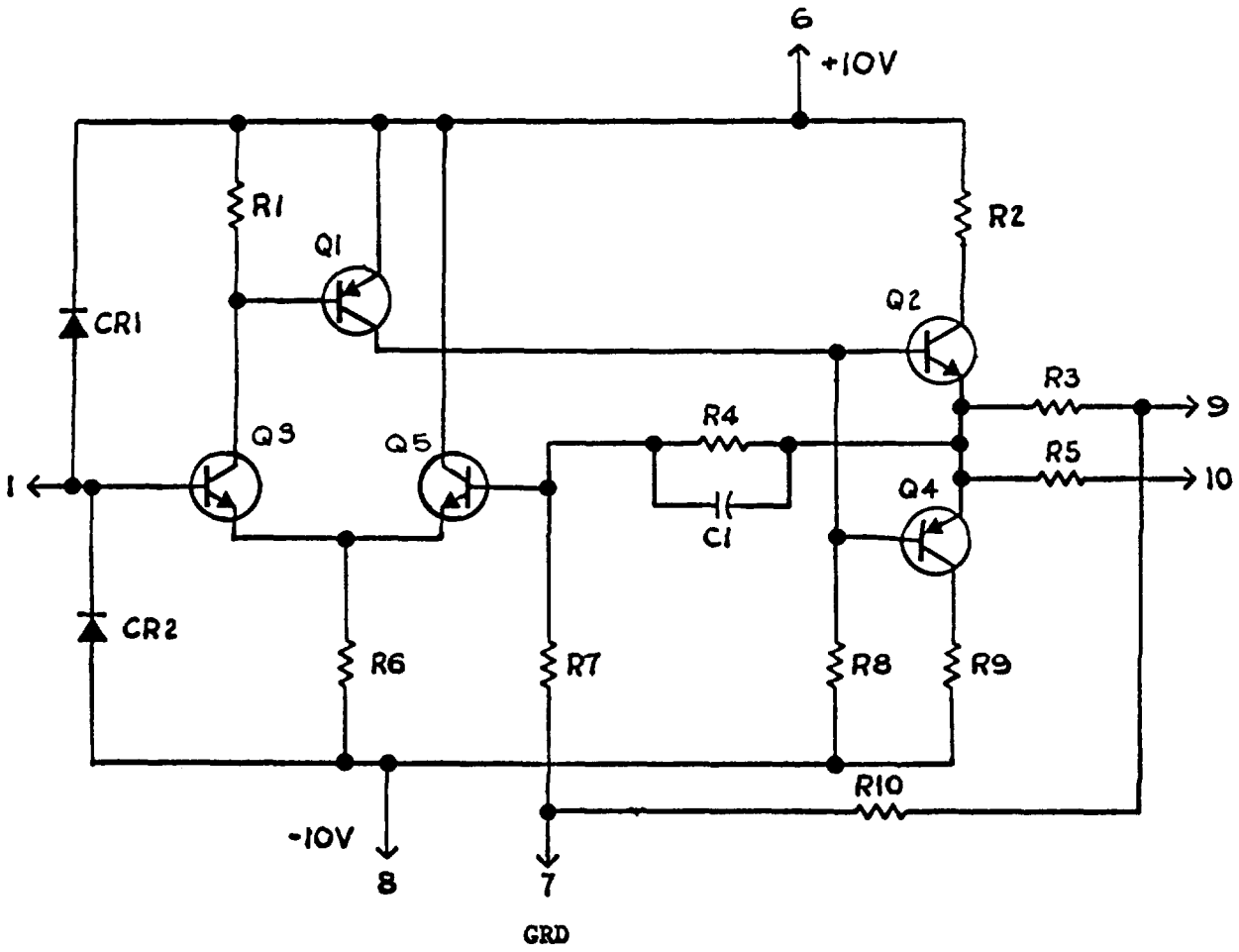


Figure 5-8. Hi-Z Input (Module 112467)

The Hi-Z Input module is designed to provide a high input impedance while supplying drive signal to the Threshold Detector module and the vertical signal to the A-Scan.

Transistors Q3 and Q5 form a differential amplifier with input from pin 1 and a feedback from the output provided by R4 and C1. Transistor Q1 inverts the signal at the collector of Q3 and drives the complementary emitter-followers QZ and Q4. These provide output signals at pins 9 and 10.

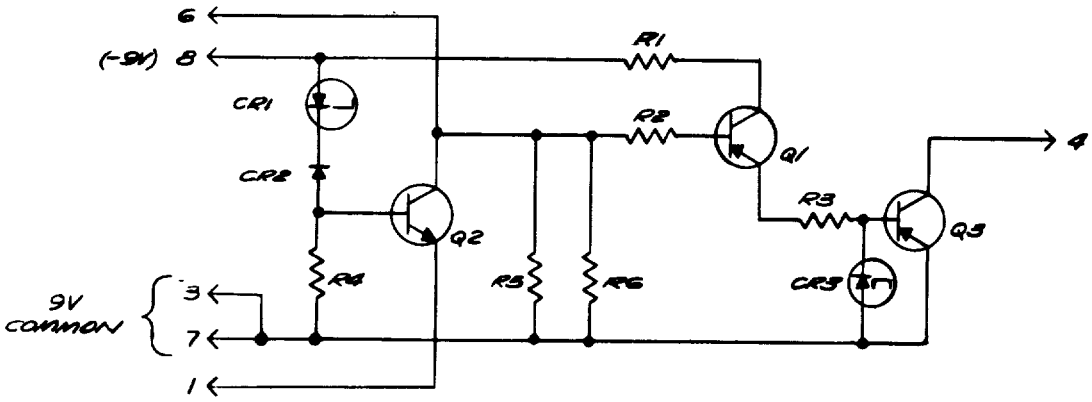


Figure 5-9. Threshold Detector (Module 514131)

The Threshold Detector module is used to sense a given current level and generate a logic level signal corresponding to the signaling current in the Analyzer input loop.

The current through Q2 and R5 and R6 is preset by an adjustment in the Input Adjust module. This establishes a voltage at the collector of Q2 which is added to or subtracted from by the voltage drop of the loop current through R5 and R6. The path of this loop current is from pin 6 through the parallel resistors R5 and R6 to pin 1.

The signal at the collector of Q2 is applied to the base of Q1, which acts as a current source for tunnel diode CR3 and the base of Q3. As the current through CR3 changes, the negative resistance characteristic causes the voltage across it to snap from one level to another, causing Q3 to be rapidly switched from one state to the other.

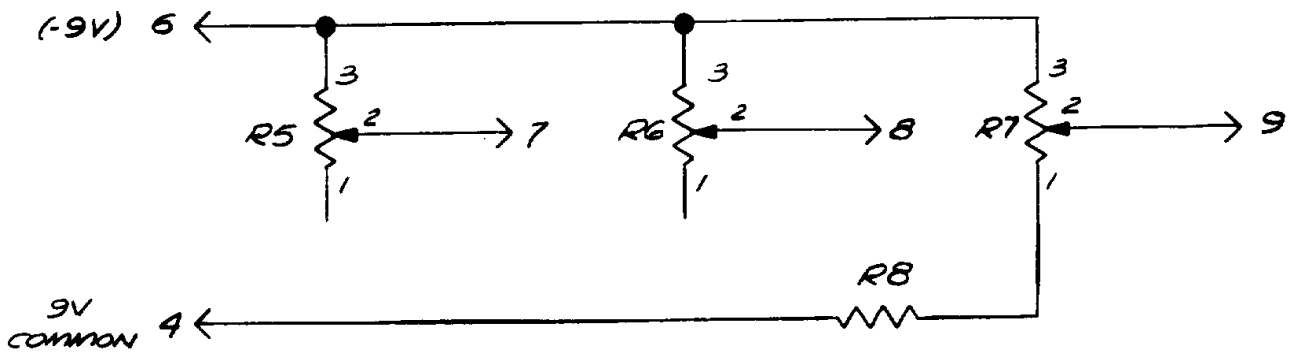


Figure 5-10. Input Adjust (Module 514154G2)

The Input Adjust module is a set of potentiometers used for initial factory calibration of the input section of the Data Analyzer.

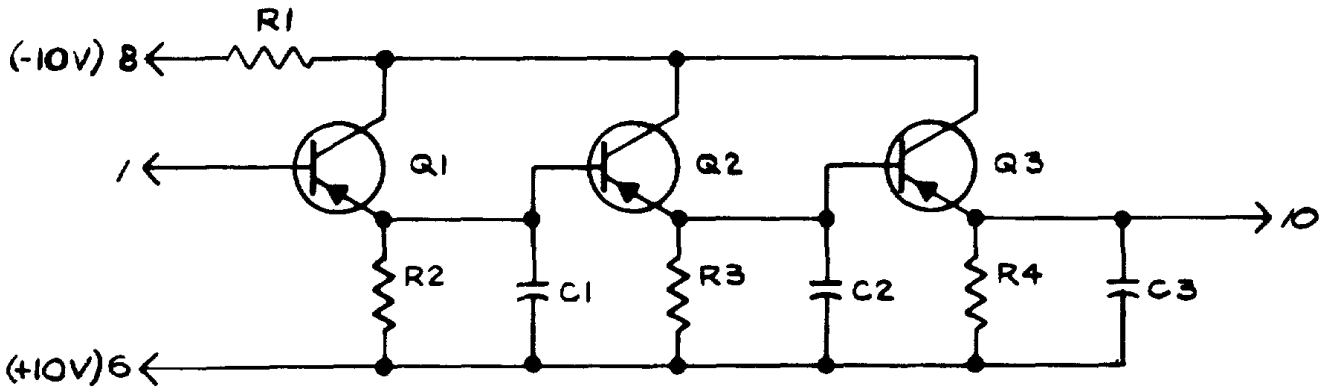


Figure 5-11. Scan Output (Module 514120)

The Scan Output module is a non-inverting buffer circuit with three emitter followers in series. The module is used to provide a low impedance output to the vertical amplifier in the A-Scan.

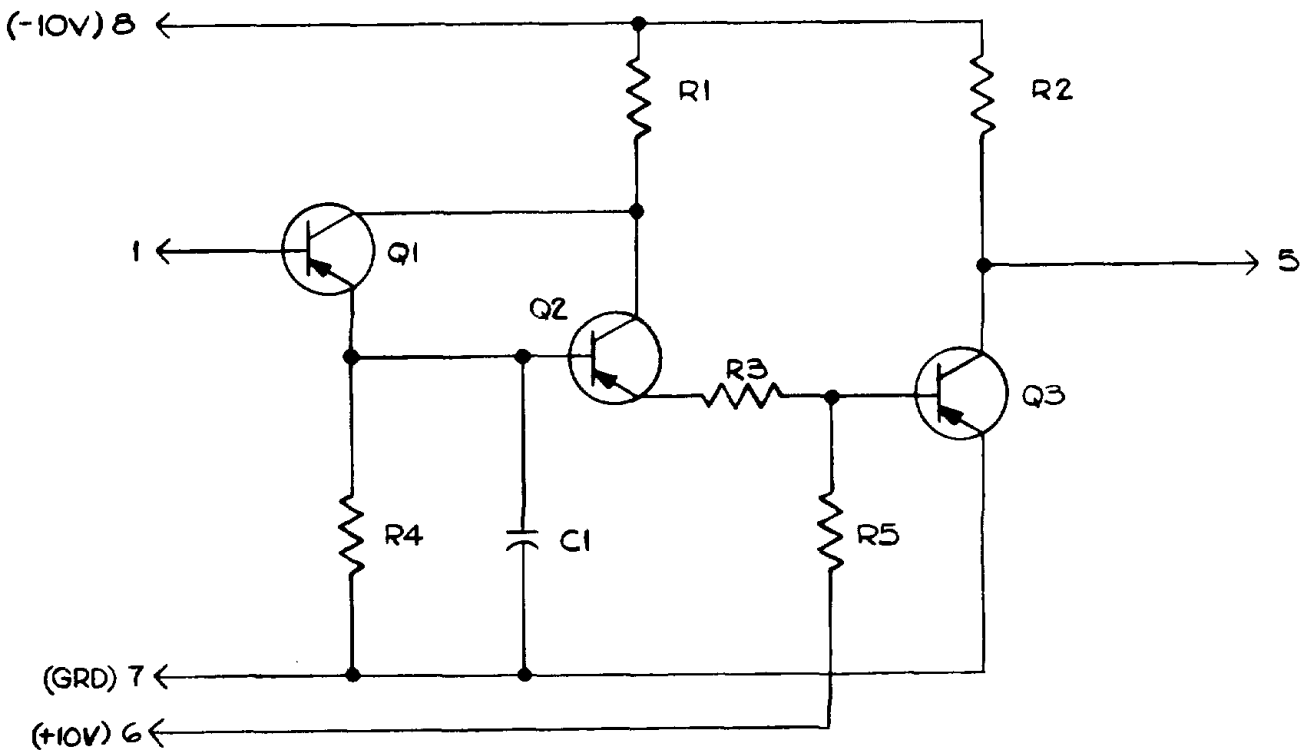


Figure 5-12. Output Switch (Module 514109)

The Output Switch module is a filter-amplifier circuit. The rectified output of the 30 mc oscillator module is filtered and amplified to normal logic levels by the Output switch.

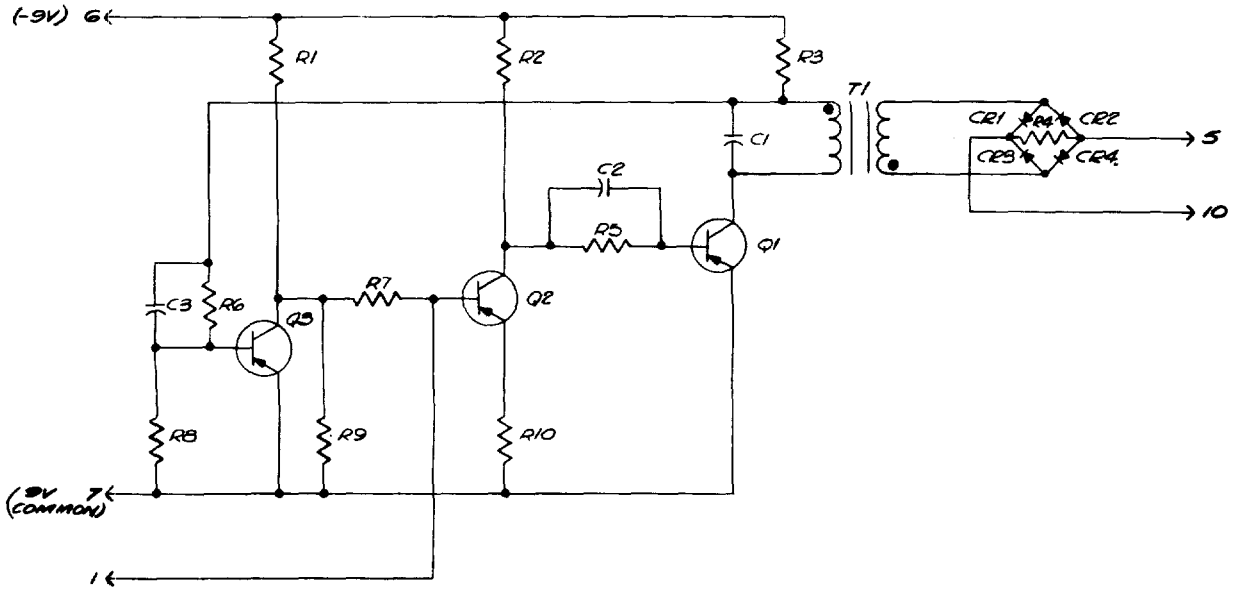


Figure 5-13. 30 MC Oscillator (Module 514121)

The 30 MC Oscillator is used to reproduce an input signal while maintaining DC isolation from its output. The oscillator uses the propagation delay of the three transistors as a frequency-determining factor. The output of Q1 is fed back to the input of Q3 by C3 and R6. The primary of T1 is tuned by C1. The output of Tl is rectified by the diode bridge composed of CR1 through CR4.

The base of Q2 is brought out to a pin for the purpose of gating the oscillator off by grounding.

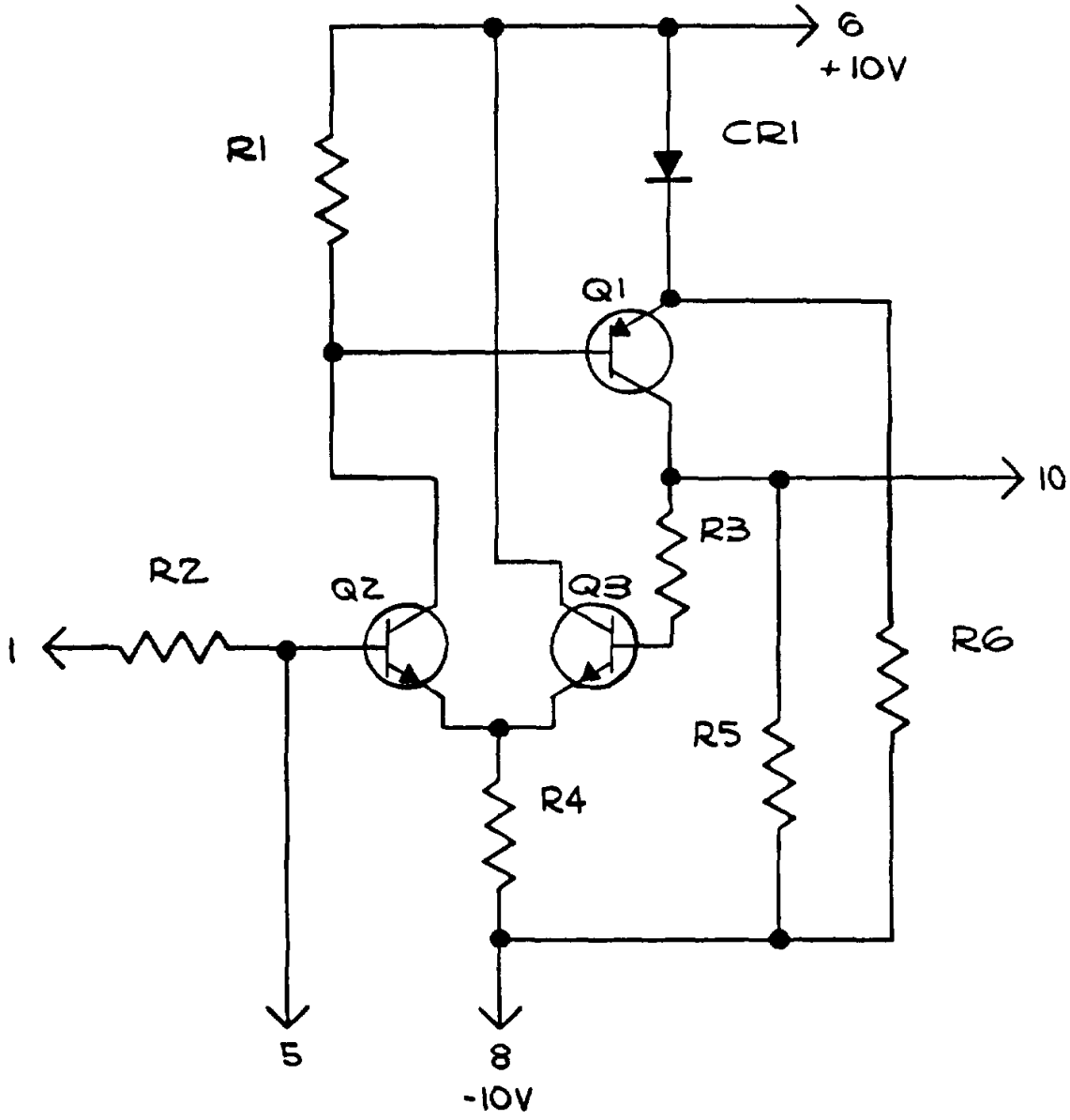


Figure 5-14. Phase Lock (Module 112482)

The Phase Lock module is used to provide DC control voltage for the voltage controlled oscillator C6A. Control signals are integrated in the base circuit of transistor Q2, which forms one half of a differential amplifier. The DC signal at the collector of Q2 is inverted and fed out to pin 10 by Q1. The output is fed back to Q3 which is the other half of the differential amplifier.

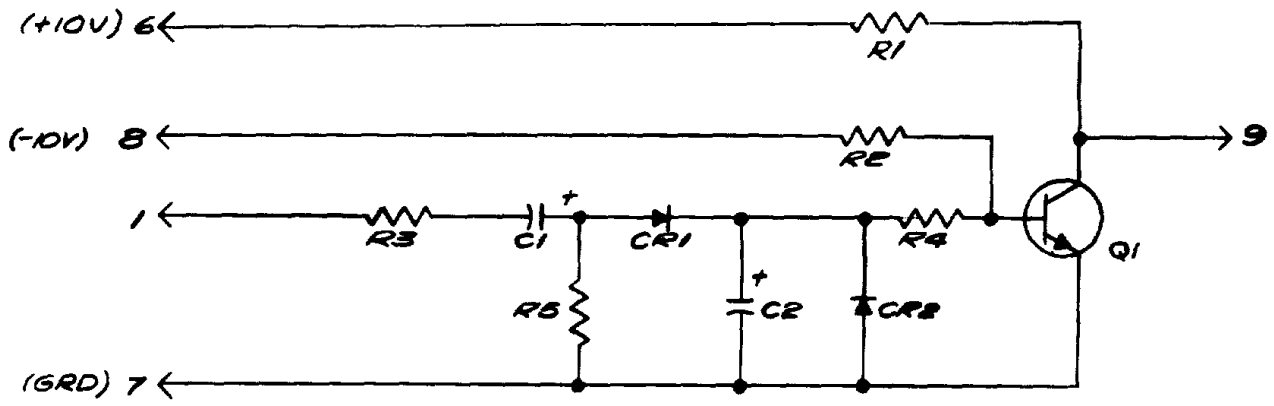


Figure 5-15. Clock Failure Detector (Module 514129)

The Clock Failure Detector input circuit integrates the squarewave input from the clock divider and uses the DC result to hold Q1 saturated, causing pin 9 to remain at 0 volts. When the input signal is removed, the negative bias turns Q1 off and pin 9 rises to +10 volts.

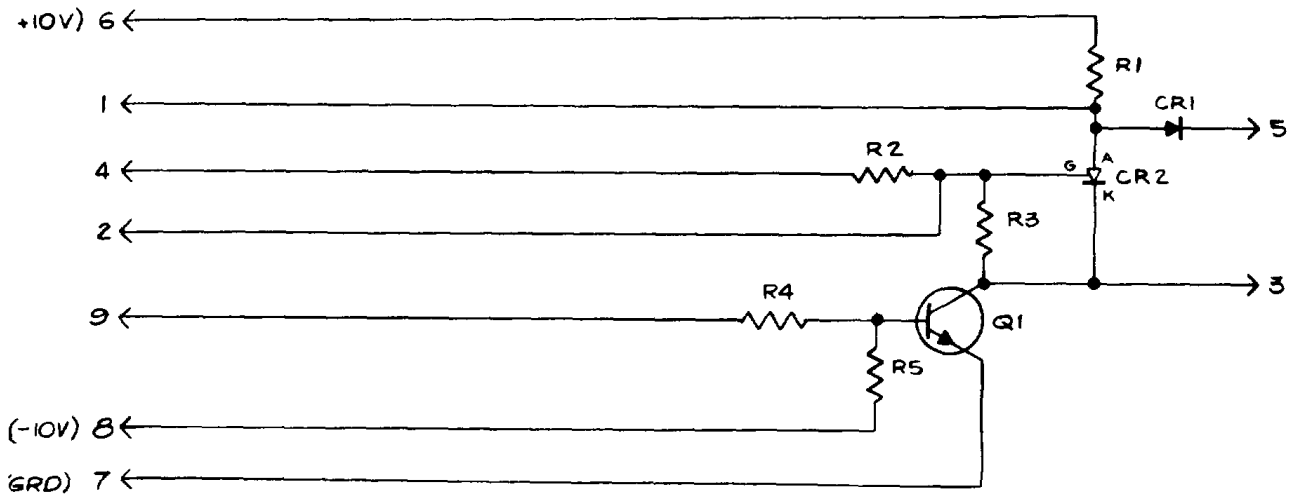


Figure 5-16. Alarm Switch (Module 514122)

The Alarm Switch module is used to turn on the audible alarm and the red "Clock Failure" indicator in the Analyzer.

A zero level at pin 9 causes Q1 to be turned off by its negative bias. A positive level at pin 9 causes Q1 to saturate. The audible alarm is connected between pin 5 and pin 3, and the "Clock Failure" indicator is connected between pin 3 and +10 volts. Therefore, when Q1 is saturated, the alarm is sounded and the indicator lighted.

Momentarily connecting pin 4 to a positive voltage causes silicon controlled rectifier CR2 to turn on, shorting out the audible alarm while allowing the indicator to remain lighted.

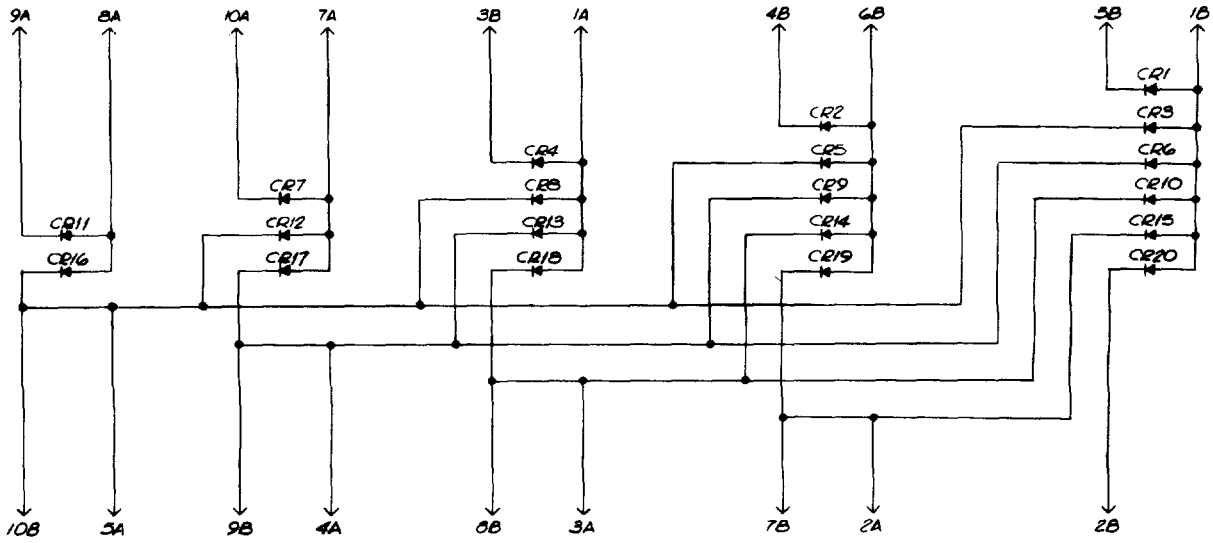


Figure 5-17. Comparator Matrix (Module 514118)

The Comparator Matrix module is a diode matrix configured to serve as a combination of negative AND gates. It is used in the digital comparator logic portion of the Analyzer to compare the contents of the output storage register with the contents of the up-down counter. A logical representation of the Comparator Matrix is shown in figure 4-2, sheet 2 of 2 of the Analyzer logic diagram page 127.

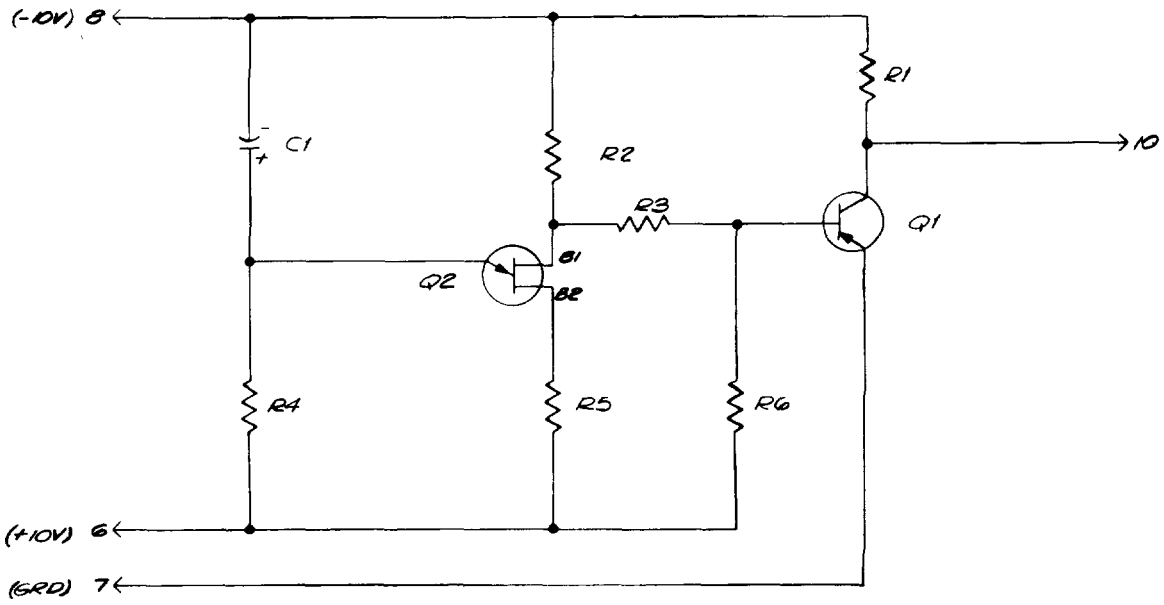


Figure 5-18. Reset Oscillator (Module 514123)

The Reset Oscillator is a low-frequency relaxation oscillator used to automatically reset the output storage register. The oscillator circuit is composed of unijunction transistor QZ and its associated components. Capacitor C1 and resistor R4 are the frequency determining elements. Transistor Q1 is an amplifier and squarer which provides a logic level pulse at the output.

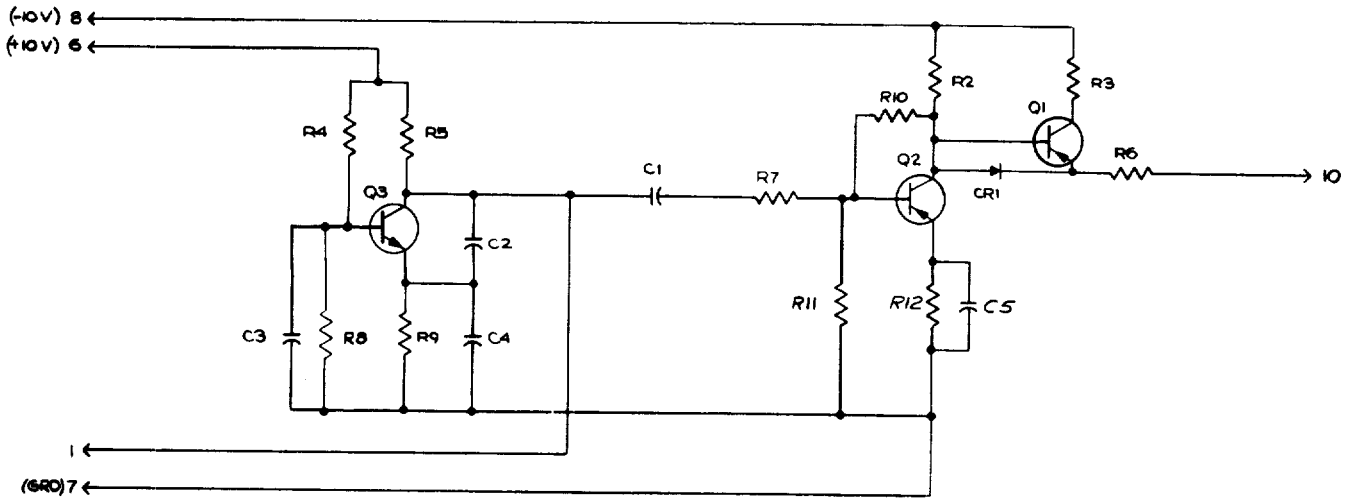


Figure 5-19. VFO (Module 514143)

The VFO module is a tunable oscillator circuit with an amplifier and an emitter follower output. The oscillator circuit is composed of transistor Q3 and its associated components. The oscillator is tuned externally by the front panel controlled tuning assembly which is connected between pin 1 and pin 7.

Transistor Q2 is an amplifier which brings the oscillator output up to logic level. Q1 is the output emitter follower.

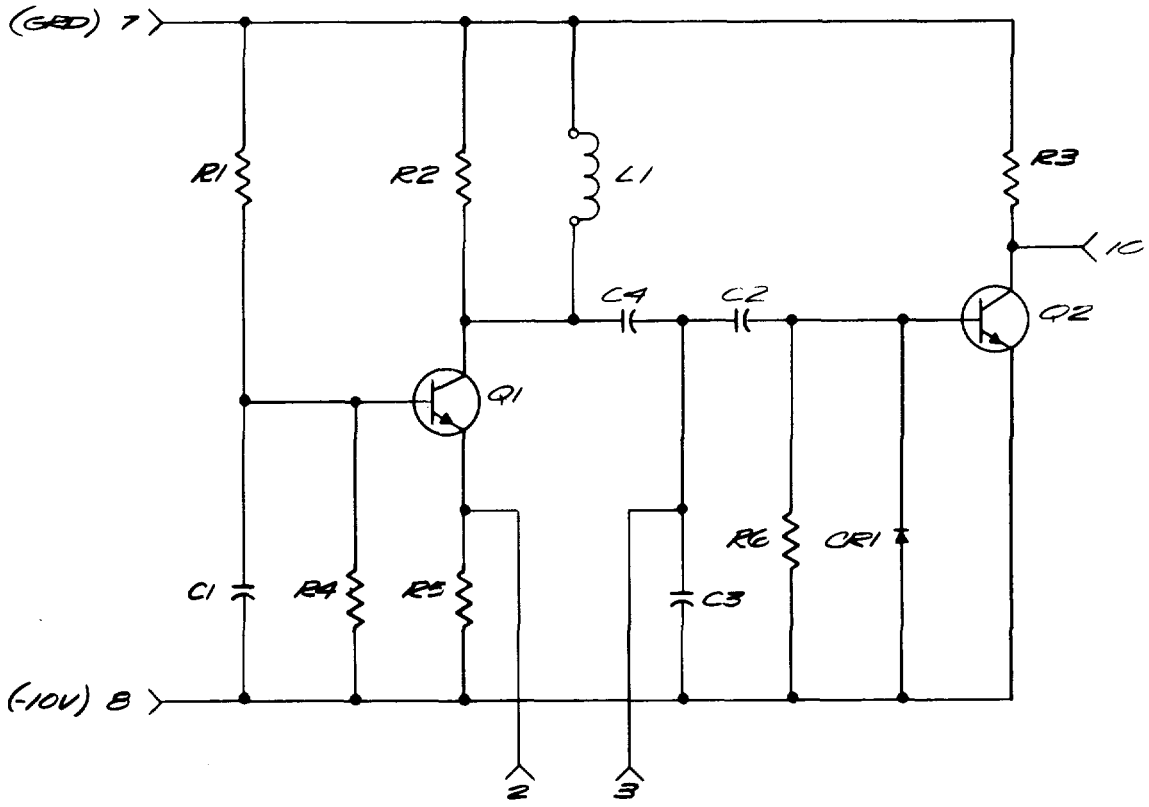


Figure 5-20. XTAL Oscillator (Module 518295)

The Xtal Oscillator is a crystal-tuned oscillator circuit which provides the basic clock signal for the Data Analyzer. The oscillator circuit is composed of transistor Q1 and its associated components and is tuned by an external crystal connected between pins 2 and 3. Transistor Q2 is an amplifier and buffer which supplies the output signal to pin 10.

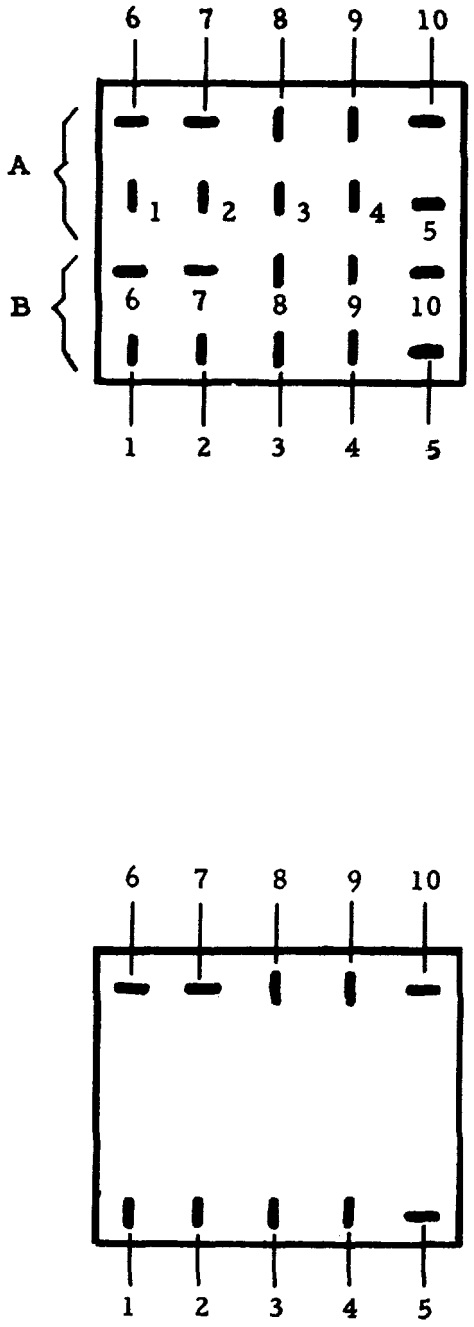


Figure 5-21. Base Diagram, Double-Size Modules

SECTION VI

MAINTENANCE

6-1. TROUBLESHOOTING PROCEDURES

Refer to part A, Section VI for system troubleshooting procedures. Refer to part A, section V for checkout procedures pertaining to the analyzer. The Data Analyzer assembly and its module locations are shown in figures 6-1 through 6-6.

6-2. ADJUSTMENT OF -5-VOLT REGULATOR MODULE

a. Coarse adjust control R6 (fig. 2-3) is adjusted for a -5-volt dc output voltage between pin 5 and ground.

b. Fine adjust control R13 is adjusted within ±5 millivolts of the 5-volt output.

6-3. ADJUSTMENT OF +10-VOLT REGULATOR MODULE

Level control R8 (fig. 2-4) is adjusted within +0.5 volt of the 10-volt output.

6-4. SYNCHRONOUS CLOCK CENTER FREQUENCY

a. The synchronous clock center frequency is adjusted by control R11 (fig. 6-6).

b. To adjust R11, short-circuit capacitor C4 in the synchronous clock and measure the frequency at location B1E10. The frequency should be 3.84 MHz ± 0.5 percent.

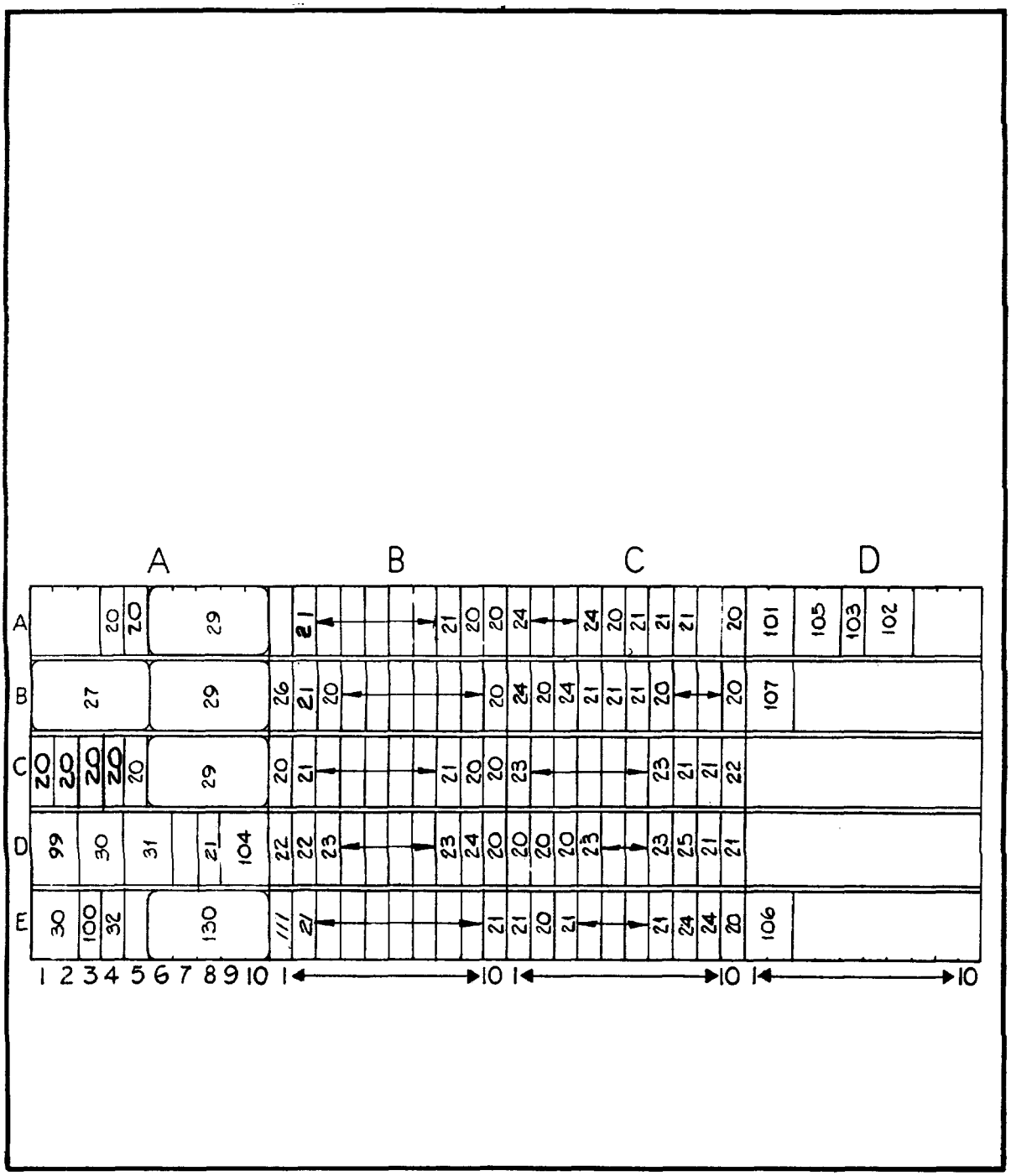


Figure 6-1. Module Locations, G1 Assembly.

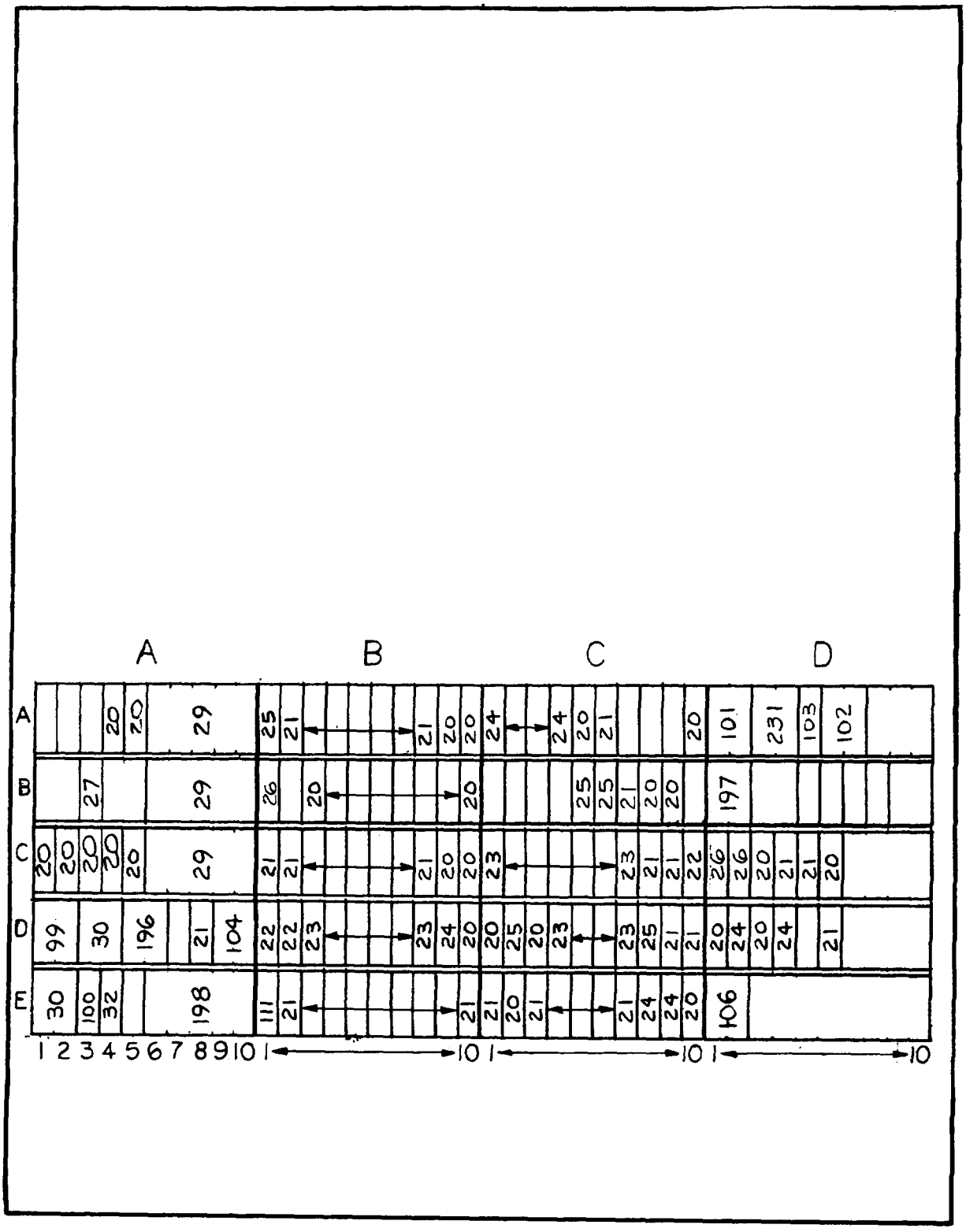


Figure 6-2. Module Locations, G3 Assembly.

Table 6-1.

MODULE IDENTIFICATION

Module Number	Module Type
20	D-NOR
21	CSR-M1
22	NOR-L
23	D/A-1 (Digital to Analog Converter)
24	NOR-M
25	BA (Buffer Amplifier)
26	DG-1 (Diode Gate)
27	-5v Reference
29	Voltage Regulator (+10v)
30	30 MC Osc
31	HI-Z Input (514130G1)
32	Output Switch
99	Scan Output
100	TD (Threshold Detector)
101	Comparator Matrix
102	Alarm Switch
103	CFD (Clock Failure Detector)
104	Reset Oscillator
105	Crystal Oscillator
106	VFO
107	Phase Lock (514125G2)
111	CSR-M
130	Input Adjust (514154G1)
196	HI-Z Input (112467G1)
197	Phase Lock (112482G1)
198	Input Adjust (514154G2)

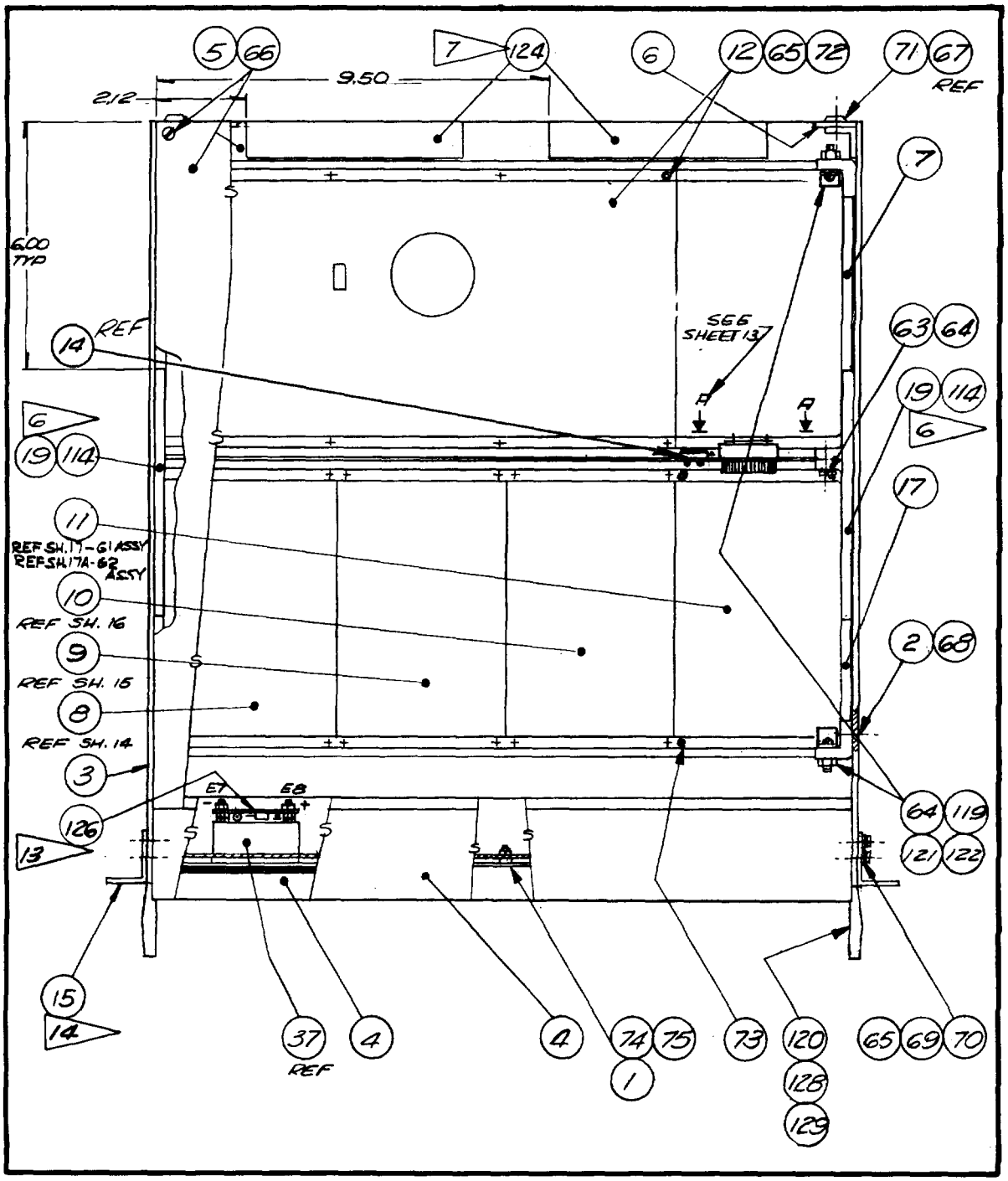


Figure 6-3. Data Analyzer Assembly, Top View.

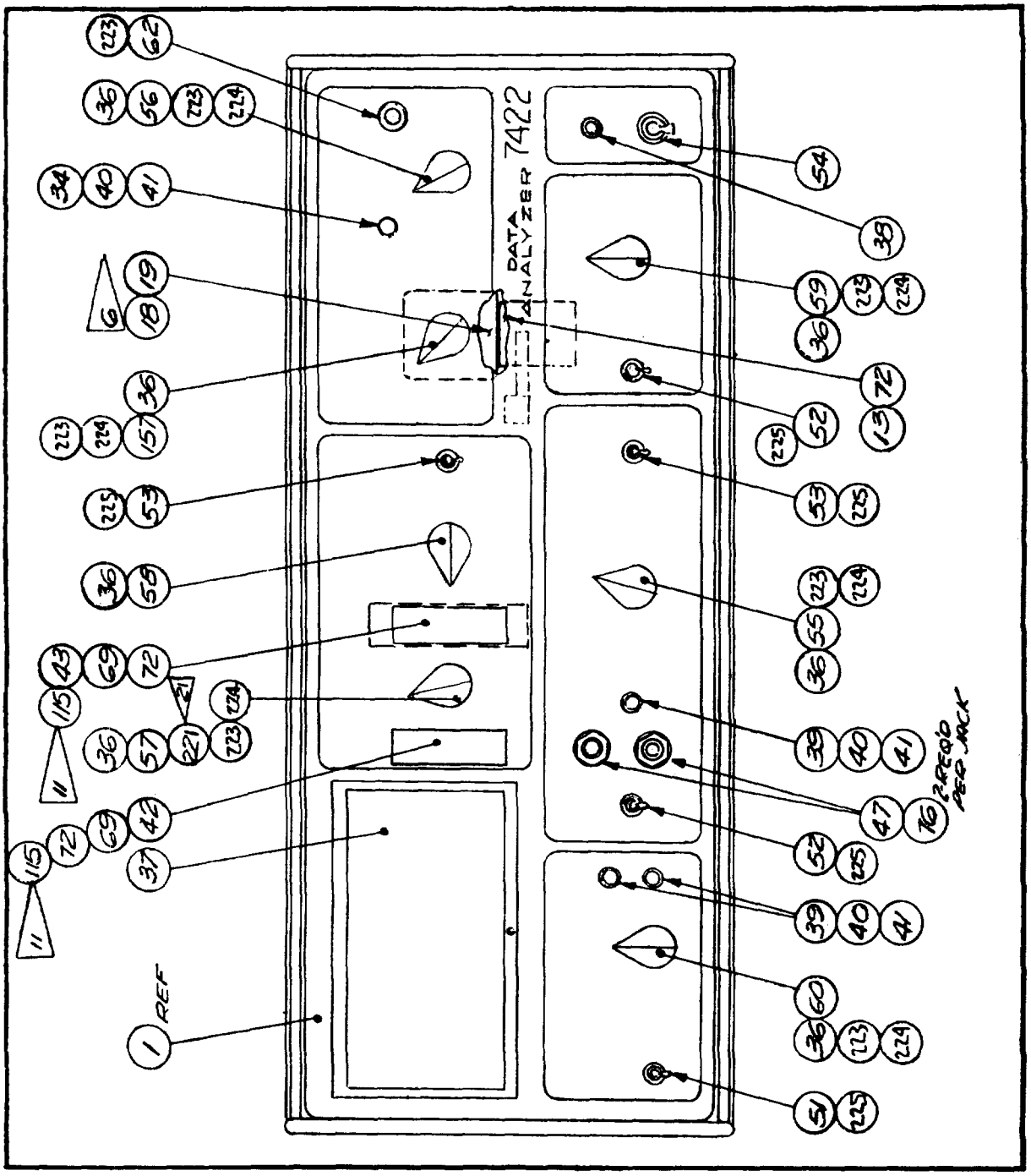


Figure 6-4. Data Analyzer Assembly, Front View.

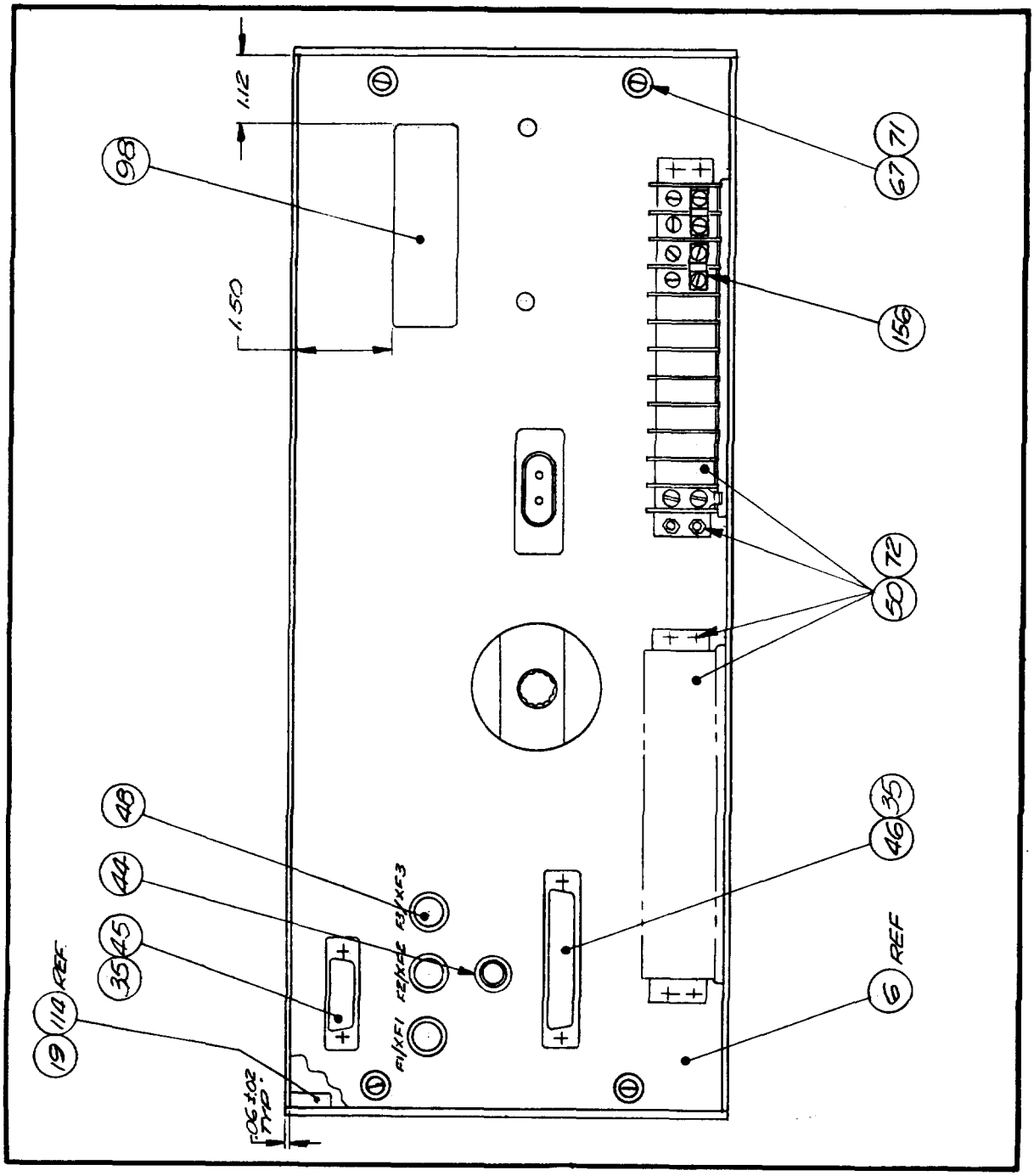


Figure 6-5. Data Analyzer Assembly, Rear View.

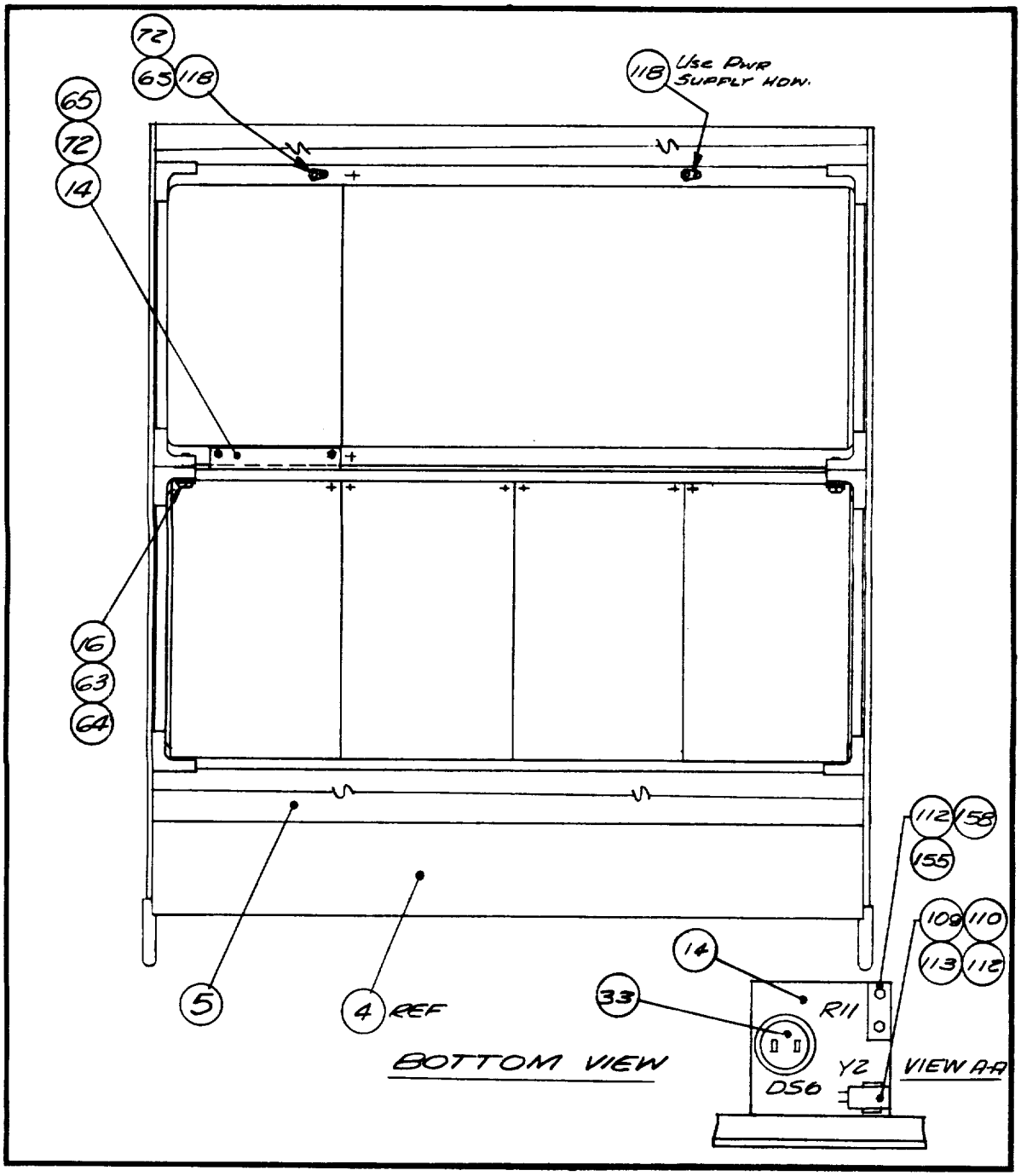


Figure 6-6. Data Analyzer Assembly, Bottom View.

SECTION VII

TIP RING SLEEVE JACK OPTION

7-1. BAUD RATE SWITCH

Data Analyzers containing the Tip Ring Sleeve option (TRS) will have the BAUD RATE switch changed as follows:

Position	Baud Rate (old)	Baud Rate (new)
1	45.50	45.50
2	50.00	74.20
3	55.60	96.oo
4	61.12	61.12
5	75.00	37.5

Note

Refer to figure 7-1 for wiring changes to BAUD RATE switch S6.

7-2. TIP RING SLEEVE JACK

Refer to figure 7-2 for wiring modifications made for the TRS jack option.

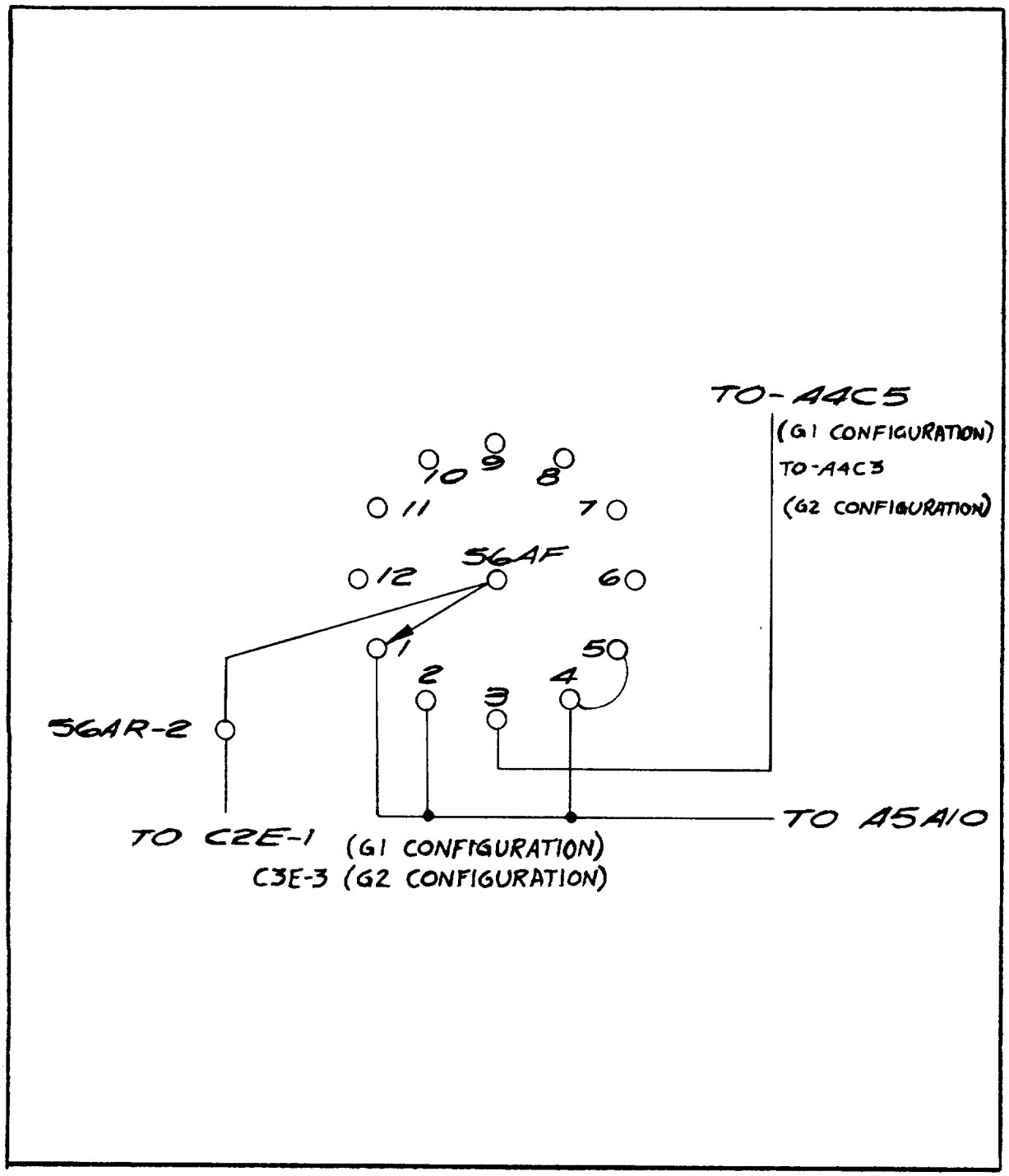


Figure 7-1. BAUD RATE switch S6 Wiring for TRS Option.

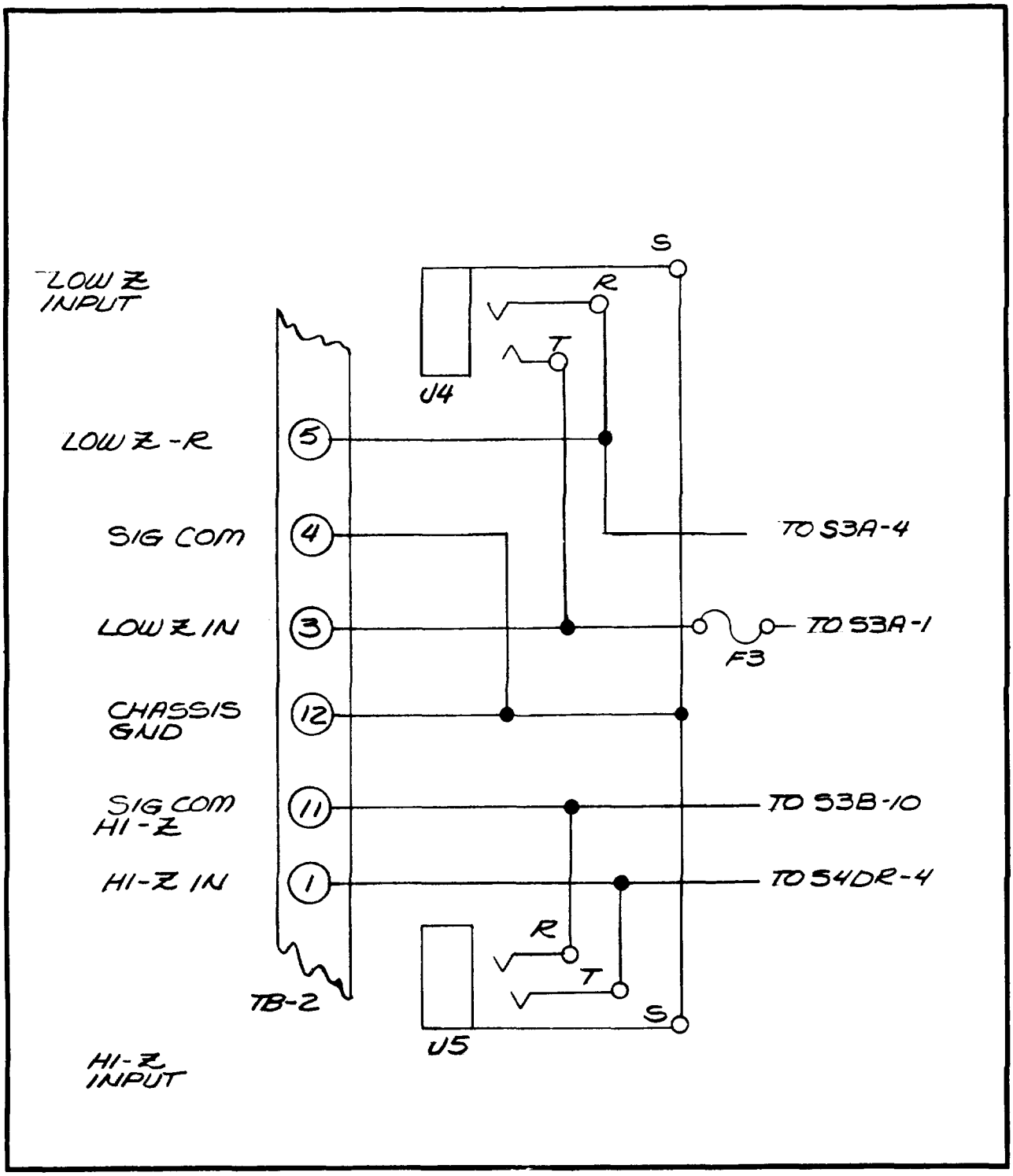


Figure 7-2. TRS Jack Wiring Modifications.

PART C
SECTION I

INTRODUCTION

1-1. GENERAL

The A-Scan, Model 7431 (figure 1-1) is a compact, transistorized unit (except for the CRT) designed for use with the Model 7422 Data Analyzer. The vertical input signal is supplied by the Analyzer, and the CRT trace is intensified to indicate the sampling points on the input waveform for distortion measurement.

When a transition is selected for analysis by the Data Analyzer, the selected transition and the associated character segment are intensified. The sampling point on the selected transition is indicated by intensification-back to normal - and back to intensification.

The A-Scan, Model 7431 is designed for use as a "slave" oscilloscope to display the signal being analyzed by the Model 7422, Data Analyzer. It cannot be used alone as it derives power and control signals from the Analyzer.

1-2. ELECTRICAL AND PHYSICAL CHARACTERISTICS

The electrical and physical characteristics of the A-Scan, Model 7431, are tabulated in table 1-1.

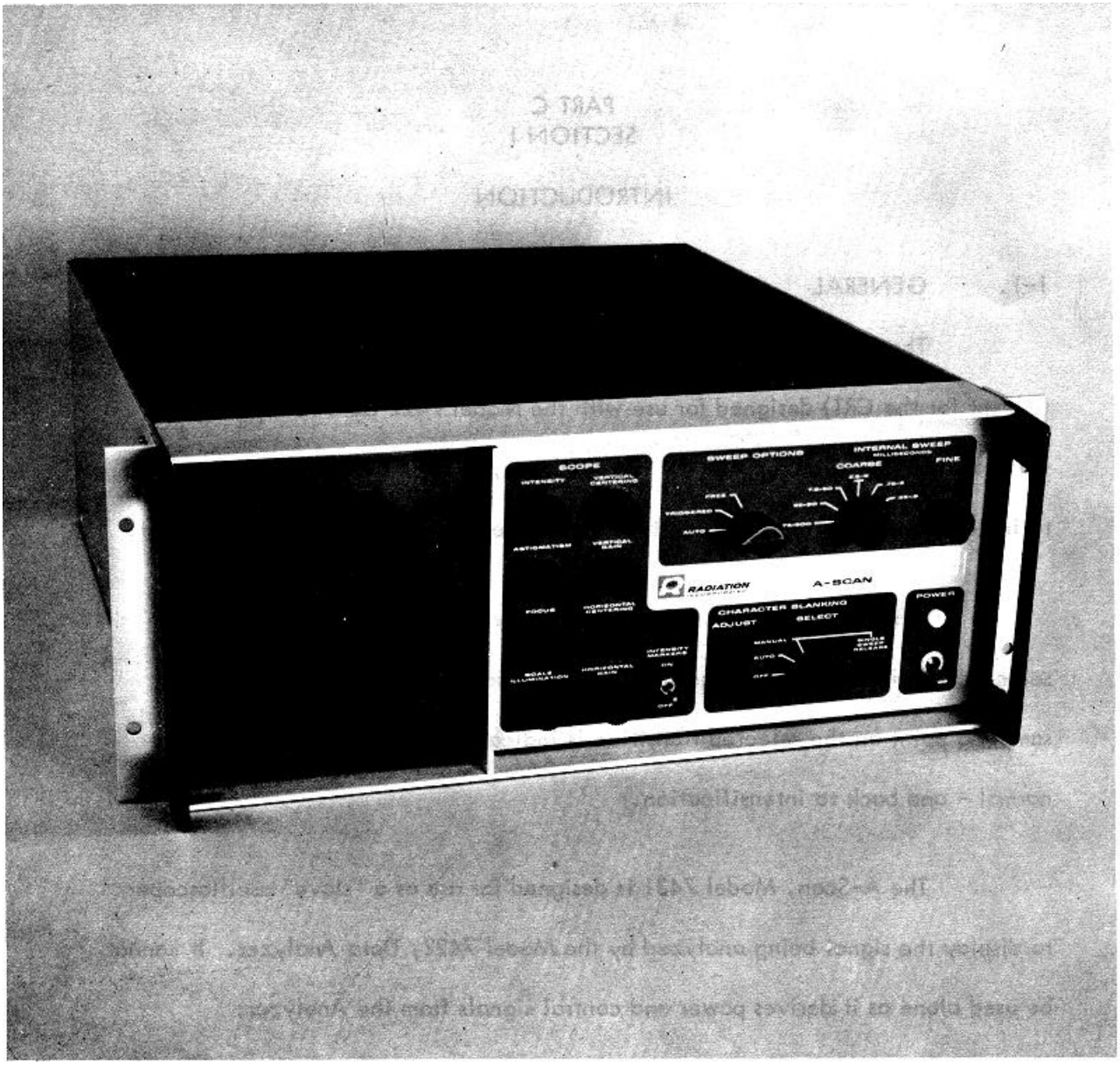


Figure 1-1. A-Scan, Model 7431 (Front View)

Table 1-1. A-Scan Model 7431 Electrical and Physical Characteristics

Vertical Input	Input supplied by Model 7422, Data Analyzer which corresponds with the input to the Analyzer.
Intensity Modulation	Trace intensified to indicate sampling points selected by Analyzer for distortion measurement. The selected transition and associated character segment are intensified. Sampling point on selected transition indicated by momentary return from intensified to normal - and back to intensified.
Blanking	Direct-coupled gate signal supplied to CRT grid to blank trace during re-trace and during waiting periods. Gate signal supplied to CRT to blank display in a variable pattern selectable by front-panel controls. Single sweep may be followed by a blank display for two, three, four, five or six character-intervals or for an indefinite interval. For single display operator resets the sweep each time.

Table 1-1. (Continued)

Display	Cathode-ray tube a flat-face five-inch tube with long persistence screen (5ADP2) A graduated scale corresponding to five and eight-unit code with horizontal and vertical graduations to permit use as a current or voltage indicating device with an accuracy of ± 5%.
Power Supply	High voltage required for CRT and deflection amplifiers is produced internally. The logic level power (-10 volts and +10 volts) is obtained from power supply In the Analyzer. AC input: 115 VAC (± 10) 50 to 400 cycles, single phase.
Internal Sweep	Sweep time periods: 250 microseconds to 800 microseconds 750 microseconds to 3 milliseconds 2.5 milliseconds to 8 milliseconds

Table 1-1. (Continued)

	7.5 milliseconds to 30 milliseconds 25 milliseconds to 80 milliseconds 75 milliseconds to 300 milliseconds
	Sweep times accommodate all modulation rates from 37.5 baud to 9600 baud.
	Sweep linearity ± 2%
	Synchronization - In AUTO SWEEP OPTION Analyzer starts sawtooth at leading edge of start pulse and un-blanks CRT. Similarly, in triggered sweep option Analyzer supplies a sync pulse at the beginning of the selected character segment to permit viewing the transition that is being analyzed. In free sweep option, sweep is not synchronized.
Horizontal Input	Digital Saw - generated by Analyzer Model 7422 for start/stop signal display.
Size:	7" high standard rack mount, depth approximately 22".

Table 1-1. (Continued)

	Receptacles at rear for connection to Analyzer Model 7422. Rack mount unit weight is 35-1/2 pounds.
212	

SECTION II

INSTALLATION

2-1. GENERAL

Upon removal from the shipping carton, inspect the A-Scan for possible in-shipment damage. Report all damages in accordance with paragraph 1-3, part A.

2-2. UNPACKING

The A-Scan Unit is shipped in a reinforced packing case designed to provide maximum protection during transport and handling. No special instructions are required for unpacking; however, care should be exercised in unpacking to prevent damage to the equipment. Once unpacked, all parts of the unit should be inspected for possible damage during transit.

2-3. MECHANICAL INSTALLATION

The A-Scan is housed in a desk-top package which may be used on any flat surface, or it may be rack-mounted by use of a rack-mount adopter kit, and it may also be mounted in a special cart built by Radiation Incorporated. Directions for rack mounting are included in the kit, and it is recommended that the top and bottom covers of the A-Scan be removed to provide additional ventilation when rack mounted.

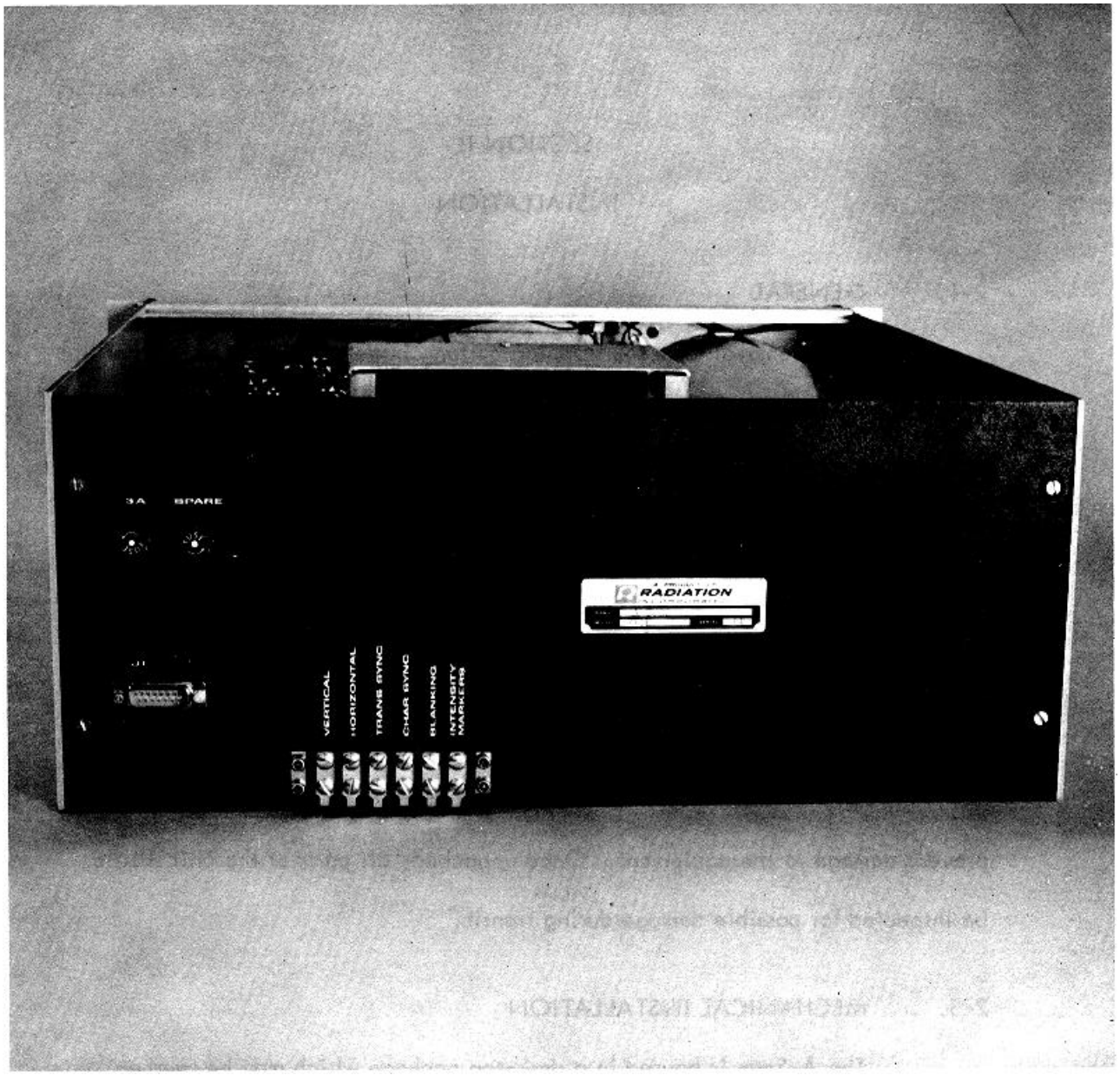


Figure 2-1. A-Scan, Model 7431 (Rear View)

2-4. ELECTRICAL INSTALLATION

The 115 volts AC 60 cps input, and the signal inputs to the A-Scan from the Analyzer are connected through a cable to connector J1 on the rear panel. (See figure 2-1)

2-5. INPUT SIGNAL CONNECTIONS

Input signal connections are tabulated in table 2-1.

A terminal board on the rear-panel of the A-Scan provides test points for major circuit tests. (These test points are placarded) (See figure 2-1).

Table 2-1. Input Signal Connections

Input Signal	Connector and Pin Number
Vertical	J1-1
+10 volts	J1-2
Horizontal	J1-3
Transition Sync	J1-4
Character Sync	J1-5
Blanking	J1-6
-10 volts	J1-7
(Not used)	J1-8
Intensity Markers	J1-9
Signal Ground	J1-10
Chassis Ground	J1-11

Table 2-1. (Continued)

115 volts AC	J1-12
115 volts AC	J1-13
115 volts AC	J1-14
115 volts AC	J1-15

SECTION III
OPERATION

3-1. GENERAL

The operation of the A-Scan is a conventional oscilloscope operation, except that it depends on the Analyzer for control signals, and power, as shown in the block diagram, figure 5-1, Part A.

CAUTION

Apply input voltages from Data Analyzer only. Maintaining high intensity for long periods of time will cause damage to internal components.

3-2. CONTROLS AND INDICATORS

The purpose and action of the controls and indicators are listed in table 3-1. For location of controls and indicators see figures 2-1, 3-1 and 3-2.

3-3. OPERATING PROCEDURES

To set the A-Scan into operation proceed as follows:

Step 1 Set INTENSITY control to its extreme counter-clockwise position.

Step 2 Set VERTICAL CENTERING, VERTICAL GAIN, HORIZONTAL GAIN, and HORIZONTAL CENTERING controls to mid-range positions.

Step 3 Set POWER switch ON. (The POWER indicator lamp should light)

Step 4 Allow one minute for A-Scan warm-up.

Step 5 Connect input signal to the Data Analyzer.

Step 6 Set A-Scan SWEEP OPTIONS switch to TRIGGERED.

Step 7 Set CHARACTER BLANKING SELECT switch to OFF.

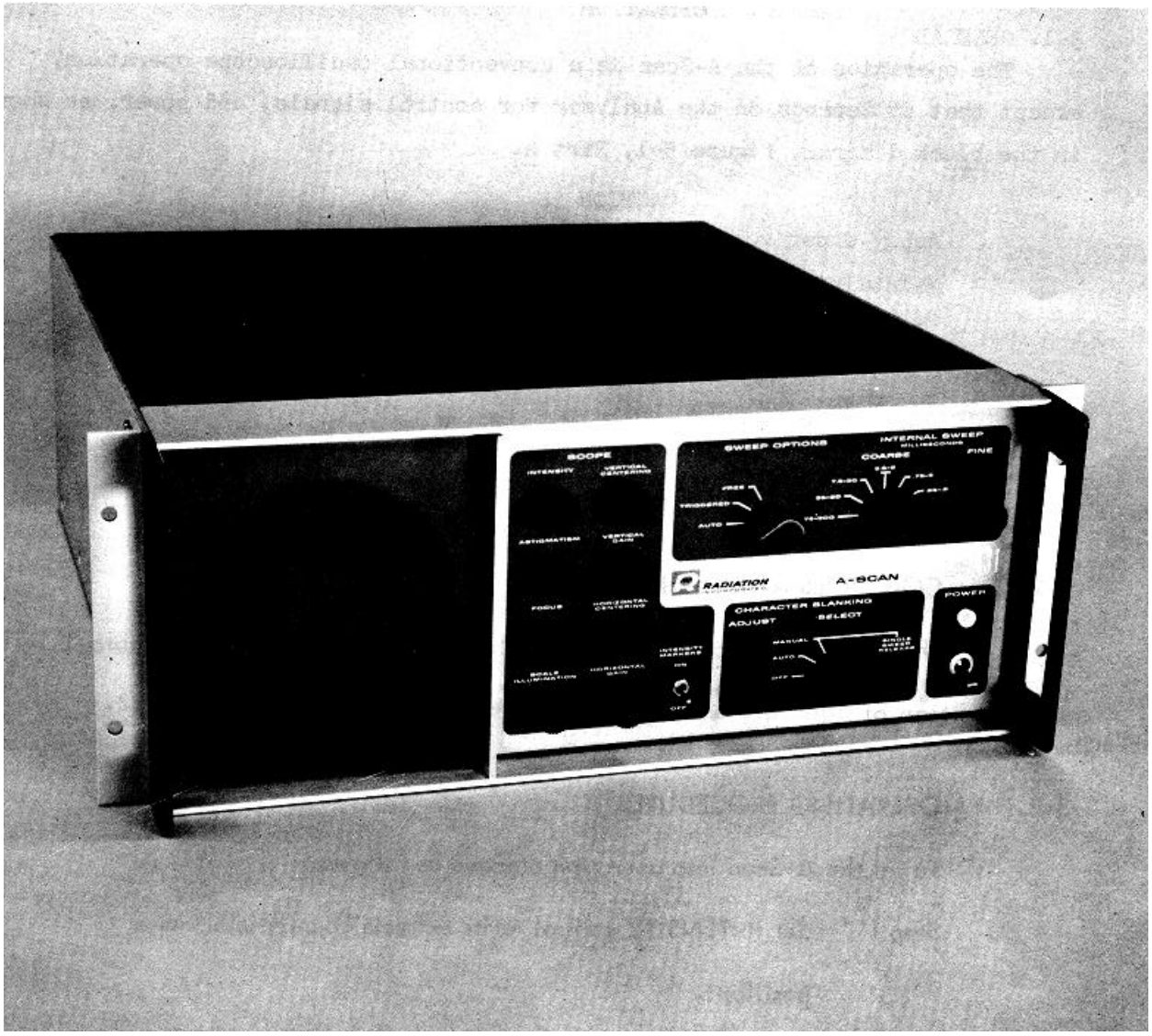


Figure 3-1. A-Scan, Model 7431 (Front View)

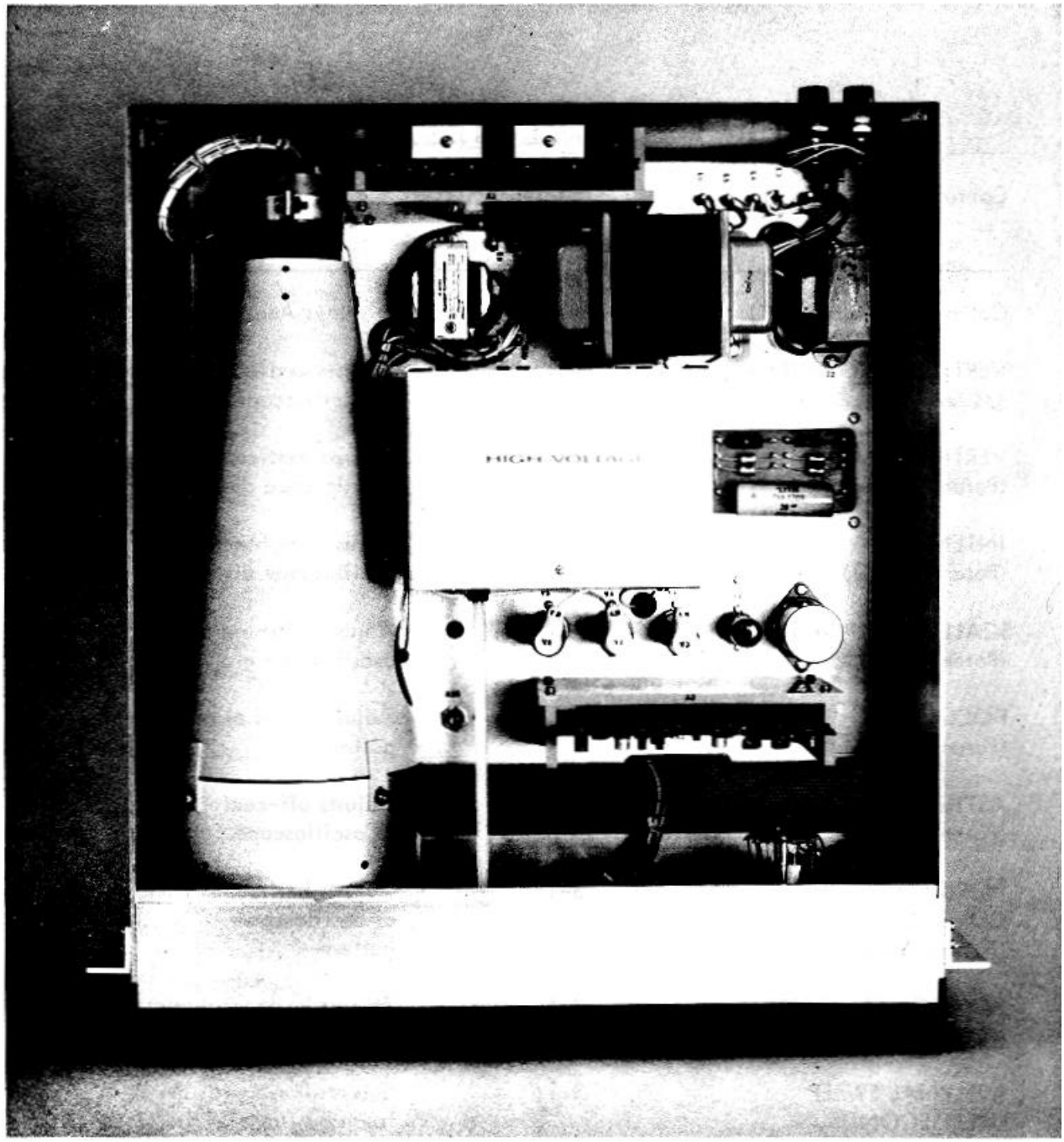


Figure 3-2. A-Scan, Model 7431 (Top View)

Table 3-1. A-Scan Controls and Indicators

Controls and Indicators	Fig. And Ref. No.	Function
Cathode Ray Tube (CRT)	3-1	Displays Analyzer input
VERTICAL CENTERING (Potentiometer)	3-1	Adjusts vertical position of oscilloscope display
VERTICAL GAIN (Potentiometer)	3-1	Adjusts vertical height of oscilloscope display
INTENSITY (Potentiometer)	3-1	Adjusts brightness of oscilloscope display
SCALE ILLUMINATION (Potentiometer)	3-1	Adjusts illumination of oscilloscope graticule
FOCUS (Potentiometer)	3-1	Adjusts focus of oscilloscope pattern
ASTIGMATISM (Potentiometer)	3-1	Adjusts off-center focus of oscilloscope pattern
HORIZONTAL CENTER RING (Potentiometer)	3-1	Adjusts horizontal position of oscilloscope pattern
HORIZONTAL GAIN (Potentiometer)	3-1	Adjusts horizontal width of oscilloscope pattern
INTERNAL SWEEP MILLISECONDS, COARSE and FINE (6 position switch and potentiometers)	3-1	Selects horizontal sweep frequency rate of the scope
SWEEP OPTIONS switch (3. position, rotary)	3-1	
- AUTO		Sets scope to display complete input character

Table 3-1. (Continued)

Controls and Indicators	Fig. And Ref. No.	Function
- TRIGGERED		Sets scope to start sweep 1/2- bit before transition selected by Analyzer TRANSITION SELECT switch.
- FREE		Sets scope to generate internal free-running sweep (non-synchronous)
CHARACTER BLANKING SELECT switch (3 position, rotary)	3-1	
- OFF		Disables blanking circuits
- AUTO		Sets scope to display one character, then blanks successive characters as adjusted by CHARACTER BLANKING ADJUST control
- MANUAL		Sets scope to unblank display during one character each time SINGLE SWEEP RELEASE switch is actuated
CHARACTER BLANKING ADJUST (Potentiometer)	3-1	Adjusts blanking interval during AUTO blanking operation
SINGLE SWEEP RELEASE switch (Non-locking push-button)	3-1	Sets scope to display a single character each time switch is depressed (when CHARACTER BLANKING switch is set to MANUALLY
POWER ON-OFF switch (Toggle- switch)	3-1	Applies AC power to scope

Table 3-1. (Continued)

Controls and Indicators	Fig. And Ref. No.	Function
POWER indicator (lamp)	3-1	Lights when power is applied to scope.
INTENSITY MARKERS switch (toggle-switch)	3-1	
- ON		Intensifies trace during transition sense period and selected character segments.
- OFF		Inhibits intensity modulation signals.

Step 8 Set INTENSITY MARKERS switch to ON.

Step 9 Rotate INTENSITY control clockwise until input signal is displayed on screen at desired brightness. (Intensity should be low enough to permit intensity pips to be seen,)

CAUTION

Never adjust INTENSITY control to cause a halo on the scope display as the CRT may be permanently damaged by burning.

Step 10 Adjust HORIZONTAL CENTERING control until pattern is centered horizontally on the screen.

Step 11 Adjust VERTICAL CENTERING control until pattern is centered vertically on the screen.

Step 12 Adjust HORIZONTAL GAIN control until the displayed pattern extends from the vertical line on the left of the screen to the vertical line of the right of the screen.

Step 13 Adjust VERTICAL GAIN control until the displayed pattern extends vertically from second horizontal graticule mark above center line to the third horizontal line below center line.

Step 14 Adjust FOCUS control until pattern near center of screen is sharp and clear.

Step 15 Adjust ASTIGMATISM control until over-all pattern is properly focused.

Step 16 Adjust SCALE ILLUMINATION control until desired brightness of graticule scale is obtained.

3-4. Automatic Character Display

In automatic character display mode the scope presents a single input signal character. For automatic character display perform steps 1 through 16 and proceed to step 17.

Step 17 Set SWEEP OPTIONS switch to AUTO.

Step 18 To view successive characters of input signal set CHARACTER BLANKING SELECT switch to OFF.

Step 19 To blank all characters for a specific time interval following display of a single character, set CHARACTER BLANKING SELECT switch to AUTO and CHARACTER BLANKING ADJUST control for desired blanking interval.

Step 20 To display a single character by manual signal, set CHARACTER BLANKING SELECT switch to MANUAL and set SINGLE SWEEP RELEASE switch each time a character is to be displayed.

Step 21 If intensified segments of the character are not desired set INTENSITY MARKERS switch to OFF.

3-5. Triggered Display

In this mode the scope is triggered at the start of the character segment selected by the TRANSITION SELECT switch on the Analyzer. The sweep speed of the scope is determined by the INTERNAL SWEEP MILLISECONDS

switch and COARSE and FINE control. To operate scope in triggered mode, proceed as follows:

Step 22 Perform steps 1 through 16.

Step 23 Set SWEEP OPTIONS switch to TRIGGERED.

Step 24 Adjust INTERNAL SWEEP MILLISECONDS COARSE and FINE controls until desired magnification is obtained.

Step 25 Set CHARACTER BLANKING switch and ADJUST control to obtain desired blanking.

3-6. FREE RUN DISPLAY

In this mode the scope sweep is triggered and generated internally. Sweep speed is controlled by INTERNAL SWEEP MILLISECONDS and COARSE and FINE controls.

Step 26 Perform steps 1 through 4.

Step 27 Set SWEEP OPTIONS switch to FREE.

Step 28 Set CHARACTER BLANKING SELECT switch to OFF.

Step 29 Adjust INTERNAL SWEEP, COARSE and FINE controls to obtain desired pattern.

SECTION IV

PRINCIPLES OF OPERATION

4-1. GENERAL

The Model 7421 "A" Scan displays the signal being analyzed by the Model 7422 Analyzer. The "A" Scan depends on the Analyzer for all control signals, and power, as shown on the block diagram (figure 4-1).

The vertical input is a voltage waveform which corresponds to the Analyzer input current or voltage. The signal is amplified by the vertical amplifier and applied to the "Y" deflection plates of the CRT.

In the AUTO SWEEP option the Analyzer generates a character-length saw starting at the leading edge of the start pulse. The signal is amplified by the horizontal amplifier and applied to the "X" deflection plates of the CRT.

When TRIGGERED and FREE SWEEP modes are selected, the saw is generated internally by the sweep circuits. In the TRIGGERED SWEEP option the Analyzer supplies a sync pulse at the beginning of the selected character segment (transition 4 is shown on the block diagram). This triggers a saw, with duration from 250 microsecond to 300 milliseconds, allowing detailed examination of the signal. The FREE SWEEP is not synchronized. The output of the sweep circuits is amplified by the horizontal amplifier and applied to the "X" deflection plates.

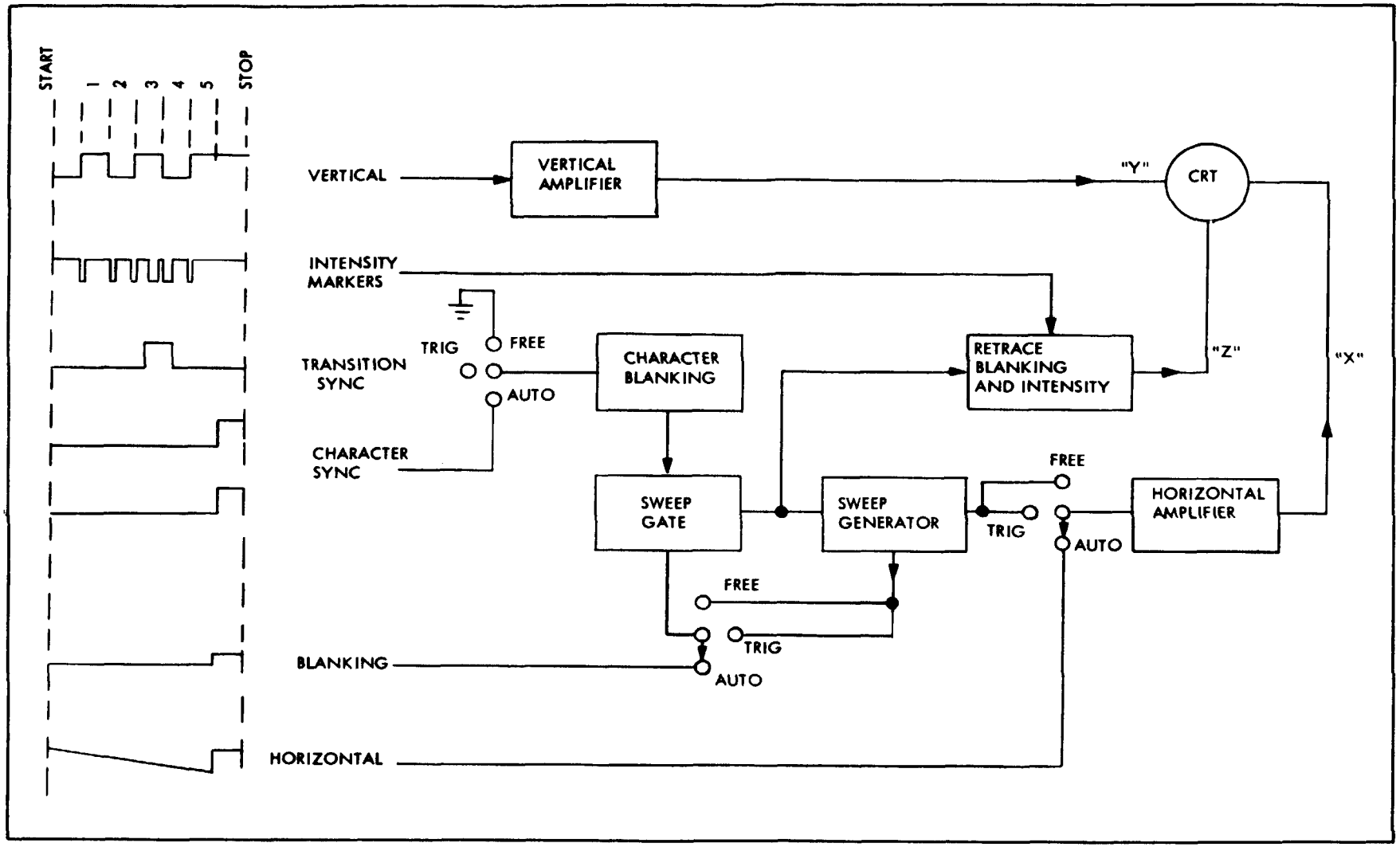


Figure 4-1. A-Scan Block Diagram

Retrace blanking in the AUTO SWEEP option is accomplished by a blanking gate generated by the Analyzer and is present during the start mark to-space transition. This signal is applied to the retrace-blanking and intensity section and blanks the CRT during retrace. When either TRIGGERED or FREE SWEEP are selected, the retrace blanking signal is fed back from the sweep generator.

Blanking of the CRT for a variable amount of time can be accomplished by the character blanking section. With the CHARACTER BLANKING SELECT switch in AUTO a single sweep may be followed by a blank display for up to two seconds. If a single sweep is desired the BLANKING SELECT switch ban be placed in MANUAL and the sweep release can be controlled by a push-button switch on the front panel.

4-2. VERTICAL AMPLIFIER

The vertical amplifier section is an emitter-follower driven differential amplifier with the output directly coupled to the vertical deflection plates of the CRT. Gain and centering are controlled on the front panel.

4-3. CHARACTER BLANKING

The character blanking output circuit is a set/reset flip-flop. It is set by the incoming signal through a NOR-gate and is reset through an AND-gate and a "one-shot" multivibrator. Blanking time is determined by the "one-shot" which can be adjusted up to two seconds.

4-4. SWEEP GATE

The sweep gate circuit is a set/reset flip-flop in the AUTO and TRIGGERED SWEEP options and a "one-shot" multivibrator in the FREE SWEEP option.

4-5. SWEEP GENERATOR

The circuit is a sawtooth generator with six discrete sweep rates and a fine-control potentiometer. The saw amplitude can be controlled by a chassis mounted potentiometer.

4-6. RETRACE BLANKING AND INTENSITY

The output of this section is a three-level signal. The signal is most positive when the intensity marker is present and nearest ground when the blanking pulse is present.

4-7. HORIZONTAL AMPLIFIER

This section is identical to the vertical amplifier described in paragraph 4-2.

4-8. SCHEMATIC DIAGRAMS

The A-Scan, Schematic Diagram, is shown in Figure 4-2. The Amplifiers, Schematic Diagram, is shown in Figure 4-3, and the Sweep Circuits, Schematic Diagram, is shown in Figure 4-4.

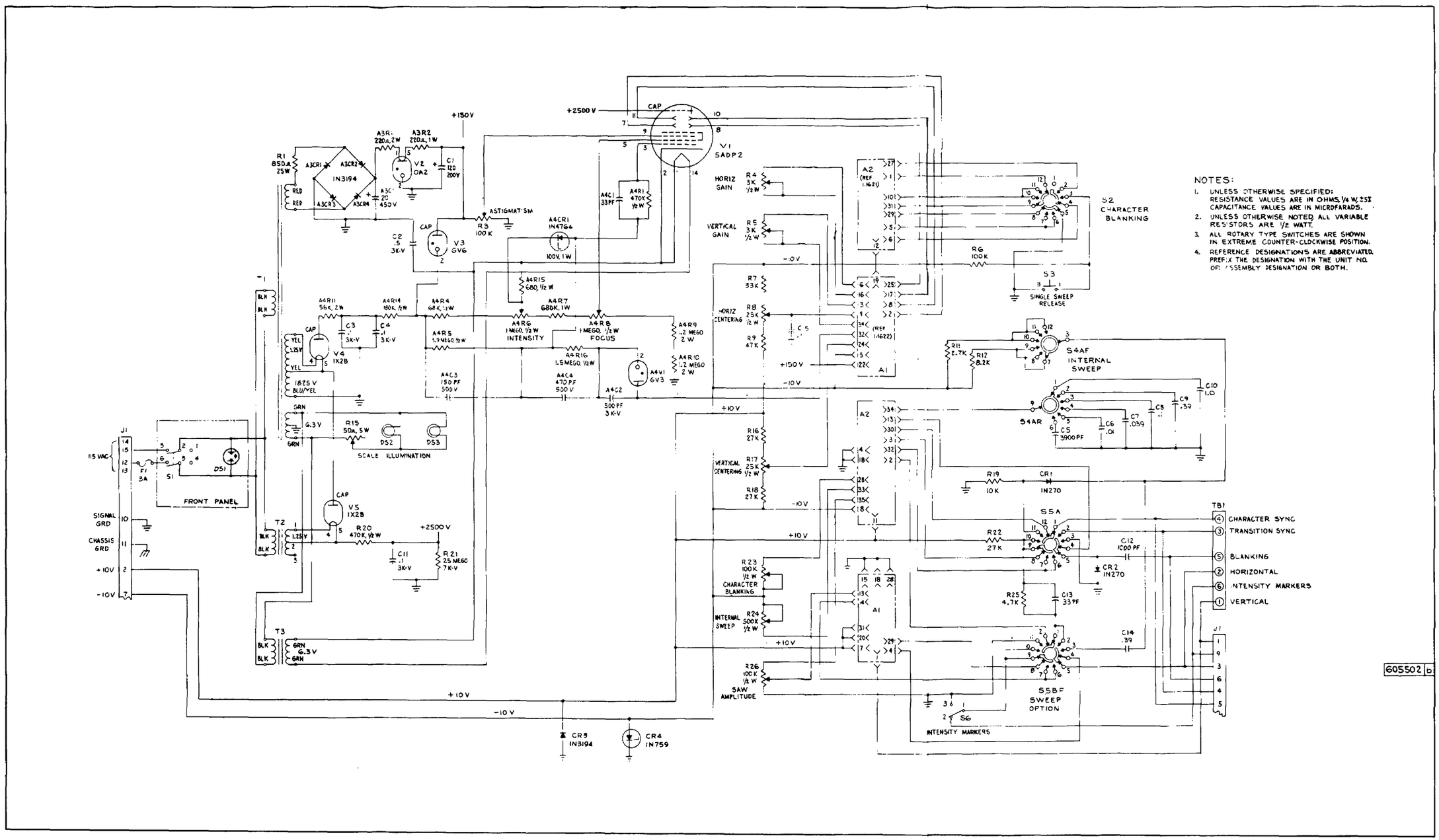


Figure 4-2. A-Scan, Schematic Diagram

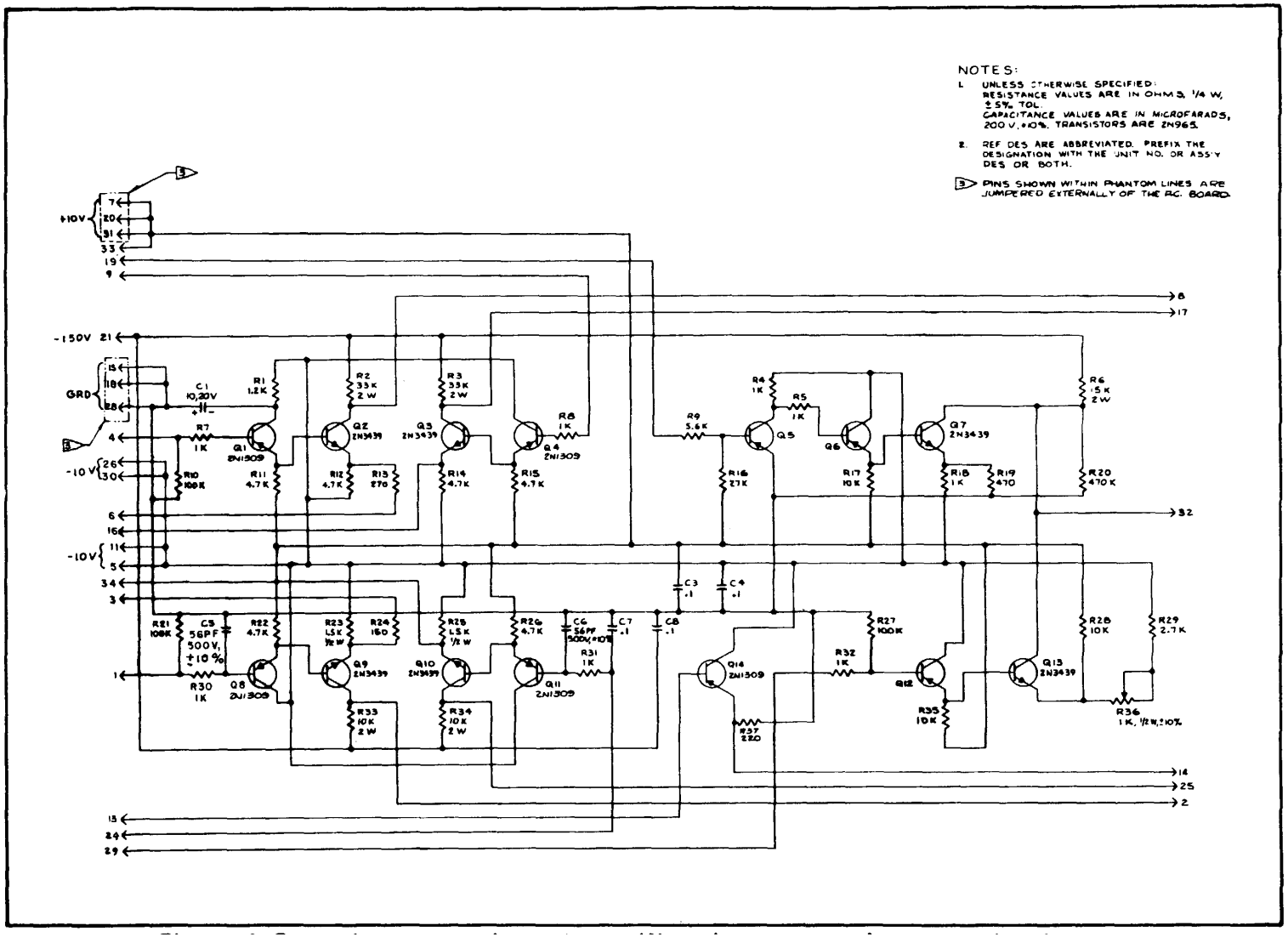


Figure 4-3. Vertical and Horizontal Amplifiers (A1 Assembly), Schematic Diagram.

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS, 1/4 W, ±5% TOL.
   CAPACITANCE VALUES ARE IN PICOFARADS.
   TRANSISTORS ARE 2N965.
2. REF DES ARE ABBREVIATED. PREFIX THE DESIGNATION WITH THE UNIT NO. OR ASS'Y DES OR BOTH.

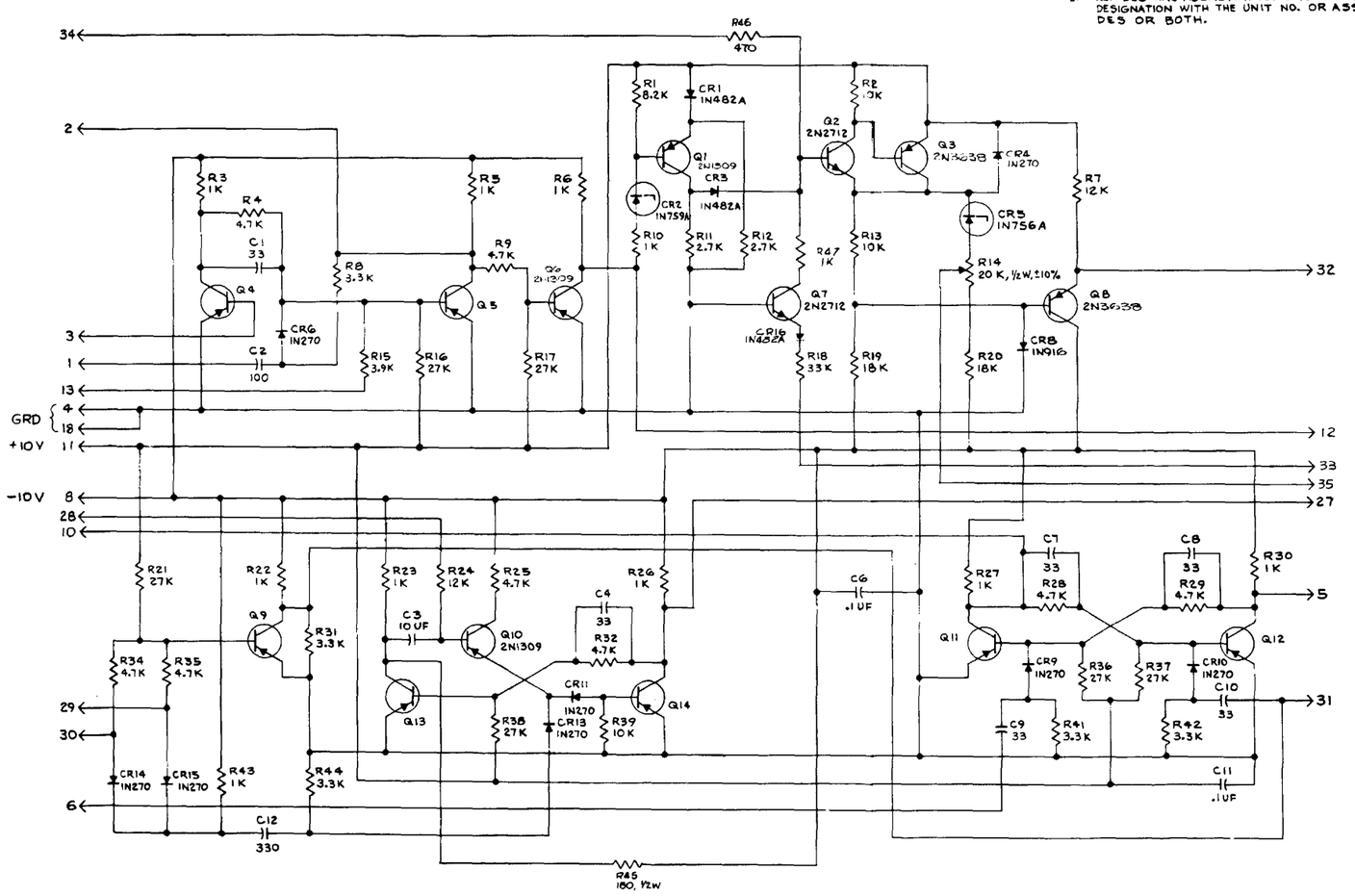


Figure 4-4. Sweep Circuit, Schematic Diagram.

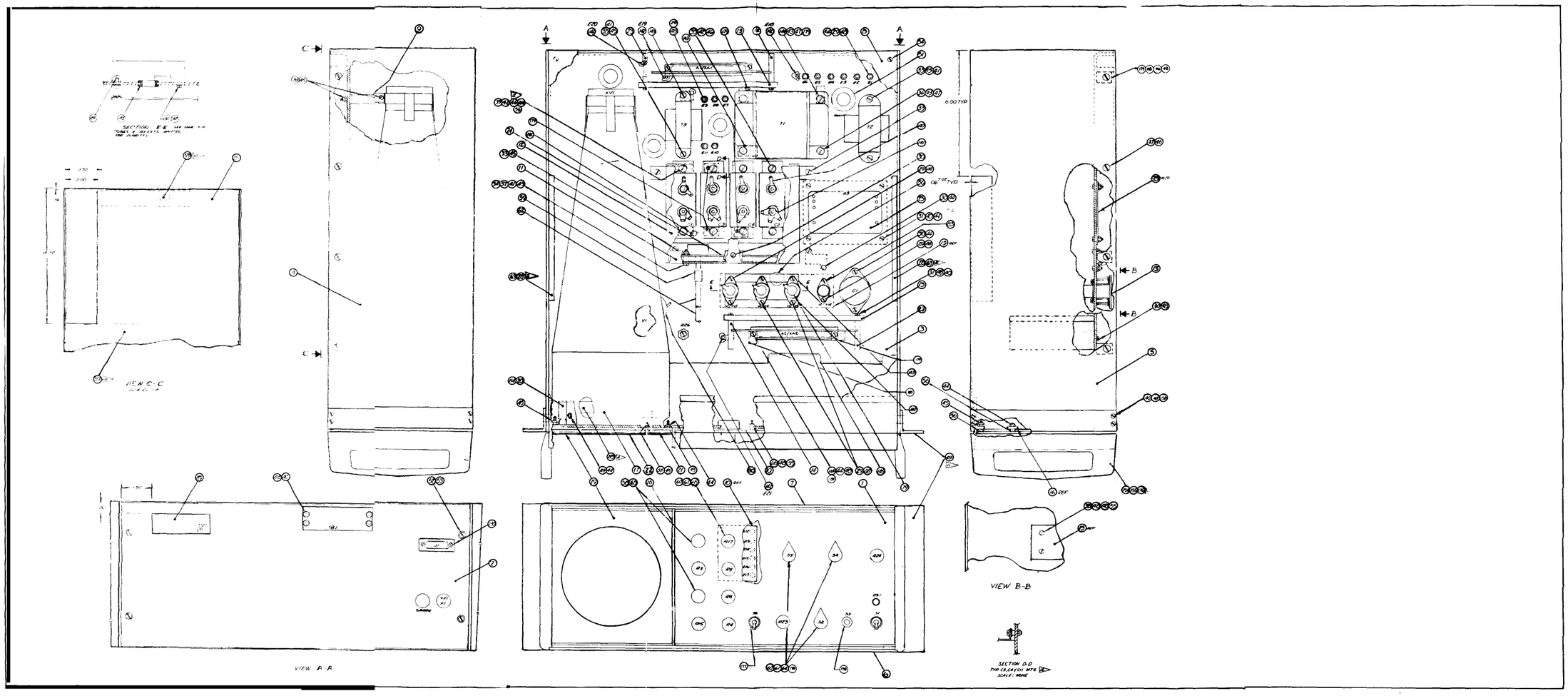


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Figure 4-5. A-Scan, Assembly

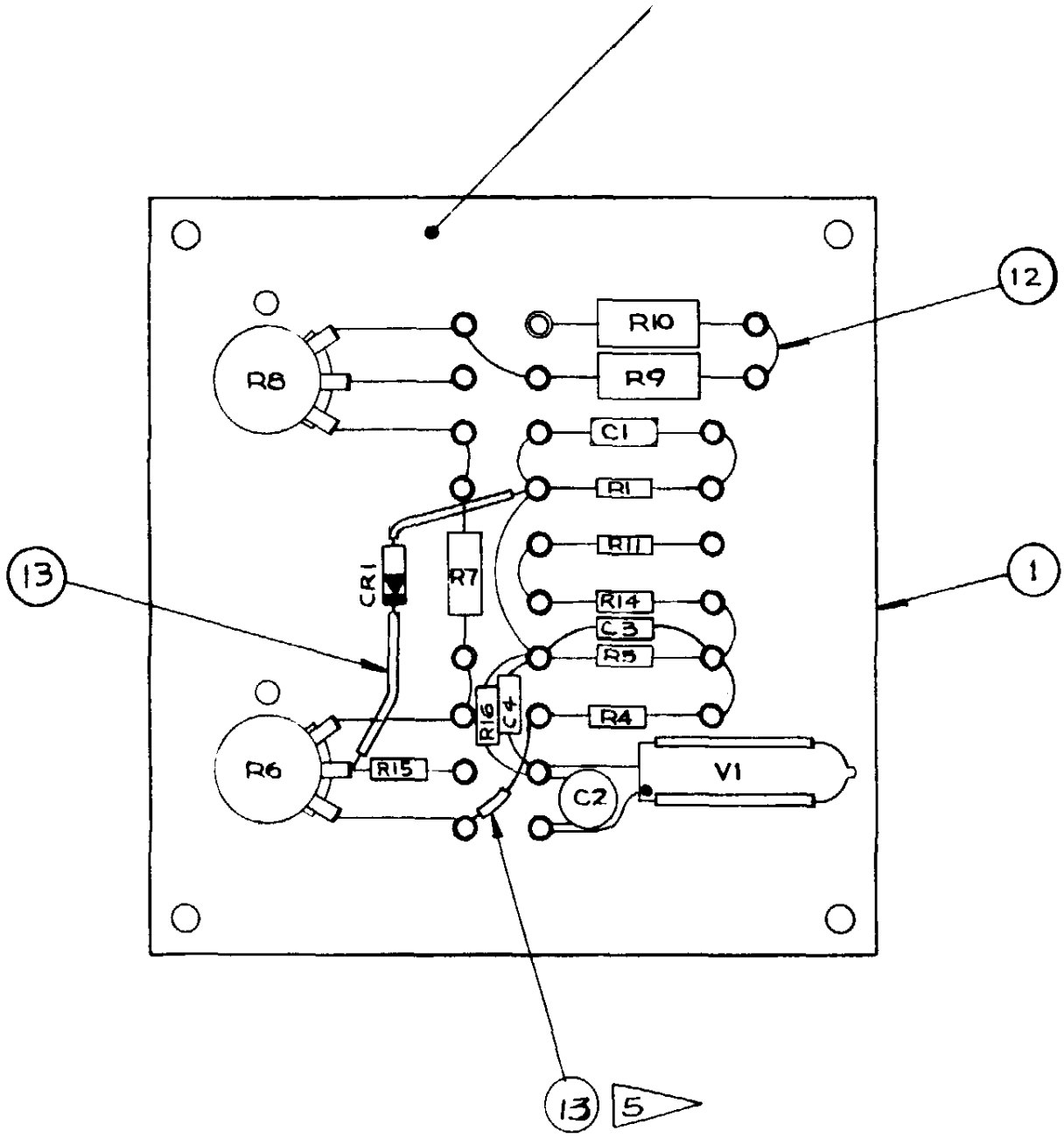

Figure 4-6. High Voltage Card, Assembly

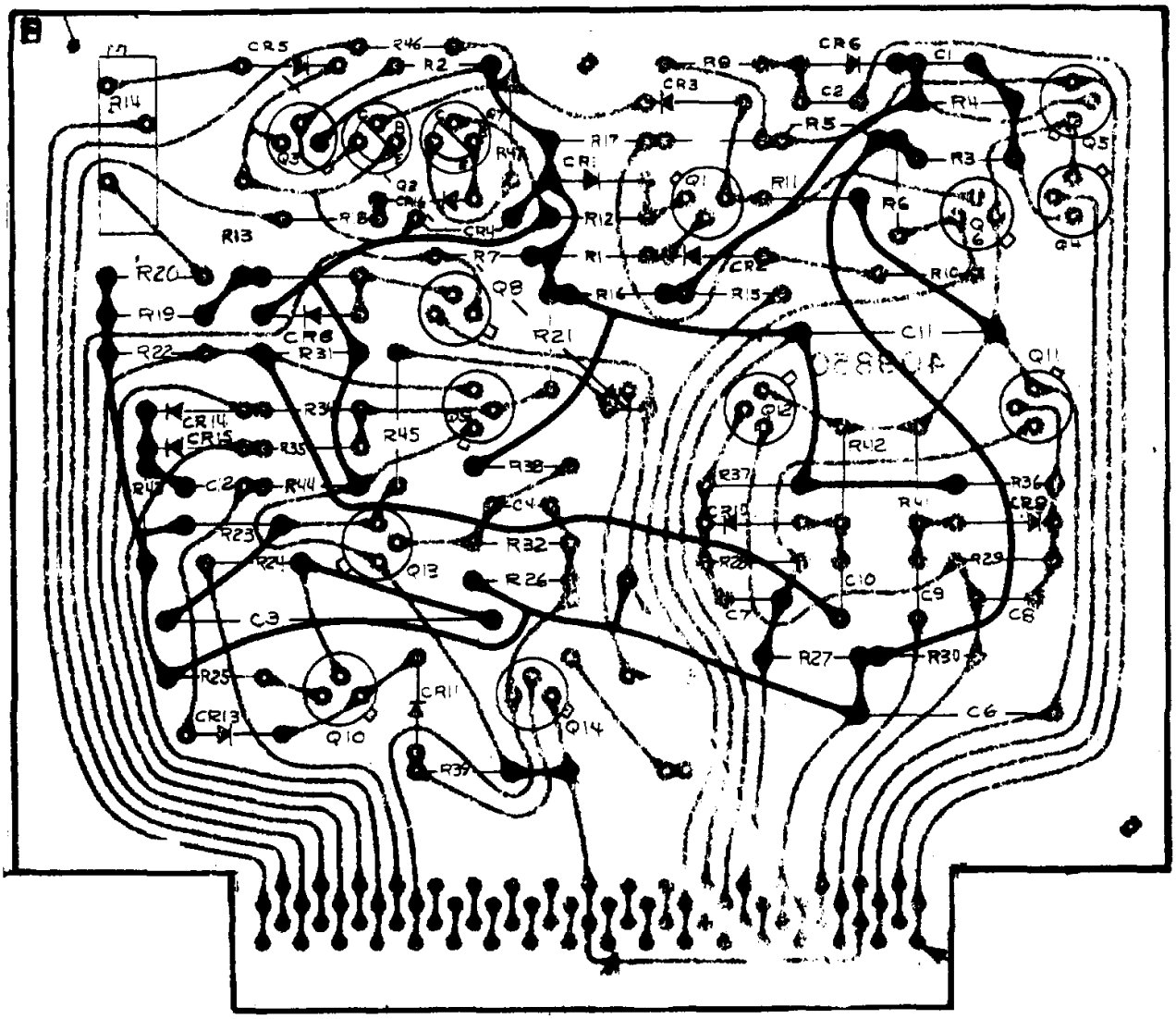

Figure 4-7. Sweep Circuit Card, Assembly A2

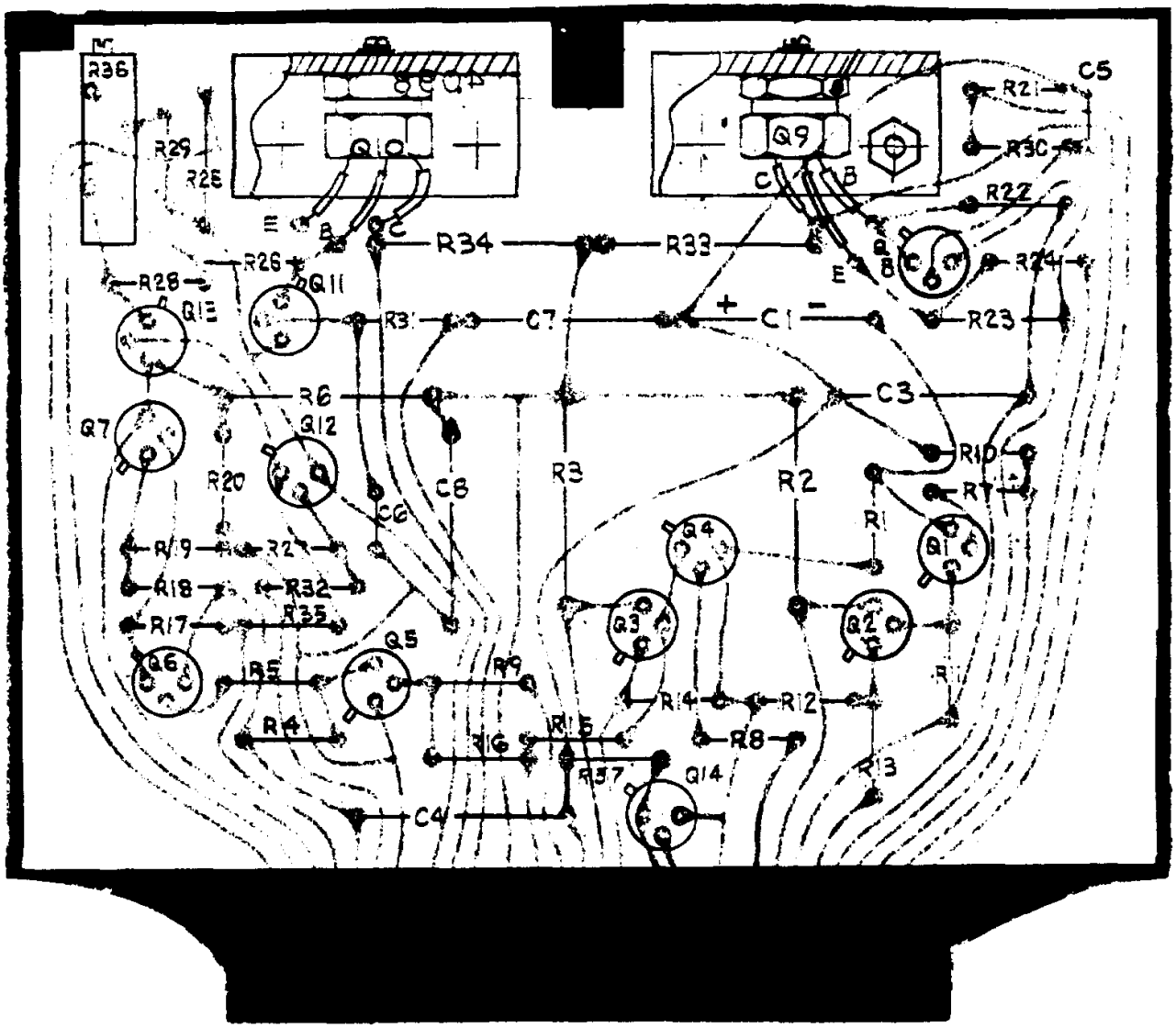

Figure 4-8. Amplifier Card, Assembly A1

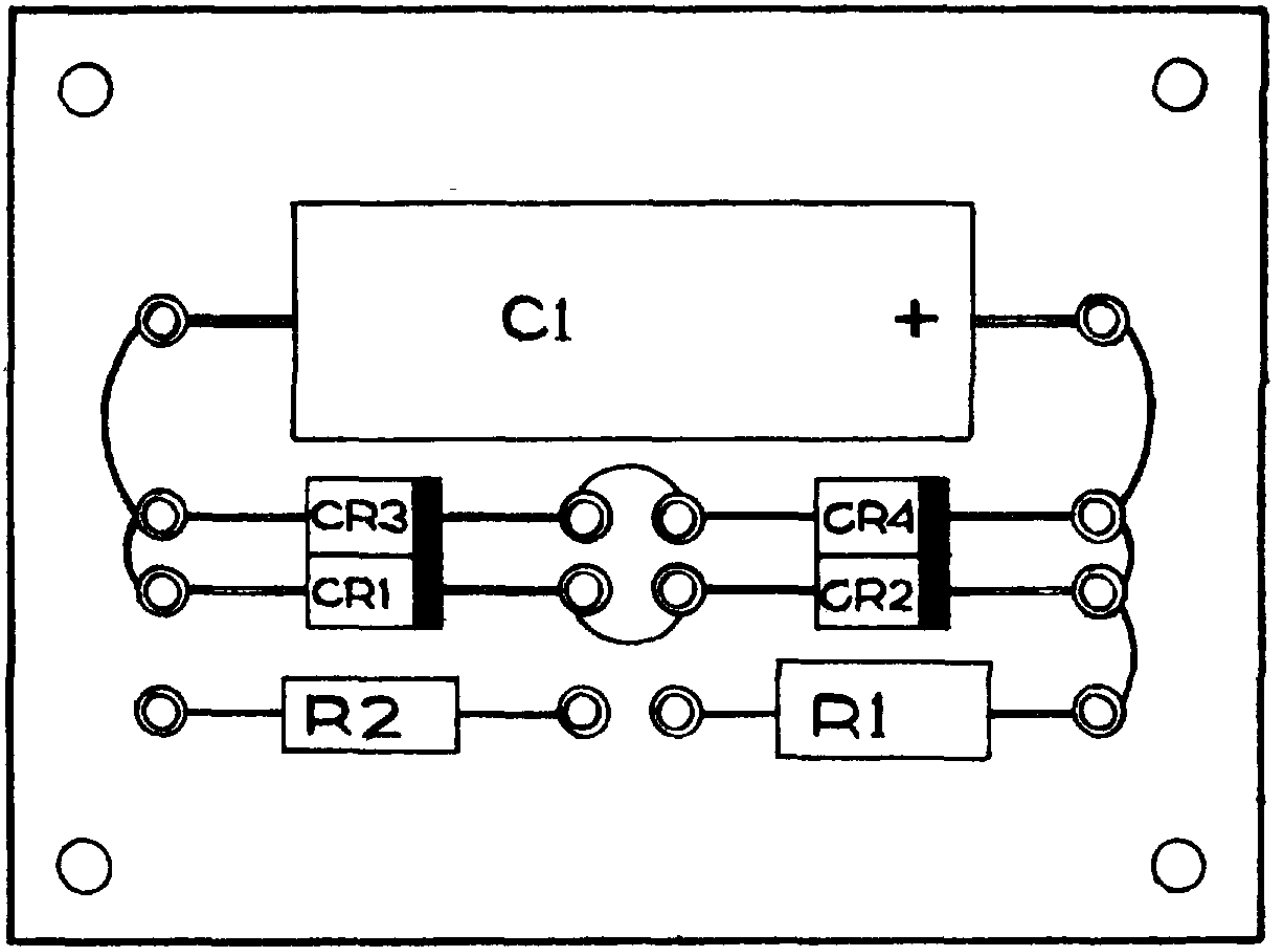

Figure 4-9. 150 Volt Card, Assembly A3

SECTION V

ADJUSTMENTS

5-1. SAWTOOTH AMPLITUDE

a. The output amplitude of the internal sawtooth can be adjusted by means of R26 located on the chassis (fig. 4-5).

b. Adjust R26 so that the sweep length is the same when the SWEEP OPTIONS switch is in the FREE position or the AUTO position.

Note
This is a field adjustment only.

5-2. INTENSITY MODULATION

a. Set the INTENSITY MARKERS switch on the A-SCAN to the ON position.
b. Set the PATTERN SELECTOR switch on the Data Transmitter to the REVERSALE position.
c. Set the TRANSITION SELECT switch on the Data Analyzer to position 1.
d. Adjust R36 on amplifier card assembly Al for best contrast between intensified transition and normal trace.

APPENDIX B

MAINTENANCE ALLOCATION

SECTION I. INTRODUCTION

B-1. General

This appendix provides a summary of the maintenance operations covered in the equipment literature for Distortion Analyzer System, Type DAS-10. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

B-2. Explanation of Format for Maintenance Allocation Chart

a. Group Number. Group numbers correspond to the reference designation prefix assigned in accordance with ASA Y32.16, Electrical and Electronics Reference Designations. They indicate the relation of listed items to the next higher assembly.

b. Component Assembly Nomenclature. This column lists the item names of component units, assemblies, subassemblies, and modules on which maintenance is authorized.

c. Maintenance Function. This column indicates the maintenance category at which performance of the specific maintenance function is authorized. Authorization to perform a function at any category also includes authorization to perform that function at higher categories. The codes used represent the various maintenance categories as follows:

Code	Maintenance Category
O	Organization Maintenance
F	Direct Support Maintenance
H	General Support Maintenance
D	Depot Maintenance

Note

When this equipment is used in a fixed station or a recoverable site, the organizational (0) and direct support (F) maintenance functions are authorized to the organization operating this equipment.

d. Tools and Equipment. The numbers appearing in this column refer to specific tools and equipment which are identified by these numbers in section III.

e. Remarks. Self explanatory.

B-3. Explanation of Format for Tool and Test Equipment Requirements

The columns in the tool and test equipment requirements chart are as follows:

a. Tools and Equipment. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool for the maintenance function.

b. Maintenance Category. The codes in this column indicate the maintenance category normally allocated the facility.

c. Nomenclature. This column lists tools, test, and maintenance equipment required to perform the maintenance functions.

d. Federal Stock Number. This column lists the Federal stock number.

e. Tool Number. Not used.

SECTION II - MAINTENANCE ALLOCATION CHART, TYPE DAS-10

MAINTENANCE ALLOCATION CHART

GROUP NUMBER	COMPONENT ASSEMBLY NOMENCLATURE	MAINTENANCE FUNCTIONS											TOOLS AND EQUIPMENT	REMARKS
		INSPECT	TEST	SERVICE	ADJUST	ALIGN	CALIBRATE	INSTALL	REPLACE	REPAIR	OVERHAUL	REBUILD		
1	DISTORTION ANALYZER SYSTEM, DAS-10	F											None	Visual
			H										1 thru 10	Operational,voltage frequency, waveforms, timing
							H						1 thru 10	Refer to procedures in Tech Manual
										H			1 thru 10	Restore to serviceable condition
1A	INDICATOR, DIGITAL DISPLAY 7431	F											None	Visual
			H										2 thru 10	Voltage, resistance, waveforms
										H			1 thru 10	Restore to serviceable condition
1A1	AMPLIFIER SUBASSEMBLY 111622G-l	H											None	Visual
			H										2,9	Voltage and resistance
								H					9	
									H				1 thru 10	Replace defective parts
1A2	SWEEP CIRCUIT SUBASSEMBLY 111629Gl	H											None	Visual
			H										2,9	Voltage and resistance
								H					9	
									H				1 thru 10	Replace defective parts
1B	INDICATOR, DISTORTION 7422	F											None	Visual
			H										1 thru 10	Voltage and resistance
									H				9	Replace plug-in modules and lamp
1B1	POWER SUPPLY 605506G4	H											None	Visual
			H										2,9	Voltage, resistance, fuse
								H					9	
									H				2,9	Replace defective parts
1C	TRANSMITTER, DIGITAL DATA 7413A	F											None	Visual
			H										1 thru 10	Operational, voltage resistance, waveforms
								H					1 thru 10	Replace defective fuse and plug-in modules

SECTION II - MAINTENANCE ALLOCATION CHART, TYPE DAS-10

MAINTENANCE ALLOCATION CHART

GROUP NUMBER	COMPONENT ASSEMBLY NOMENCLATURE	MAINTENANCE FUNCTIONS											TOOLS AND EQUIPMENT	REMARKS
		INSPECT	TEST	SERVICE	ADJUST	ALIGN	CALIBRATE	INSTALL	REPLACE	REPAIR	OVERHAUL	REBUILD		
101	BAUDOT FORMAT SUBASSEMBLY 511810G1	H	H						H	H			None 2 None 1 thru 10	Visual Voltage and resistance Replace defective parts

SECTION III - TOOL AND TEST EQUIPMENT REQUIREMENTS, MODEL DAS-10

TOOL AND TEST EQUIPMENT REQUIREMENTS

TOOLS AND EQUIP	MAINT. CATEGORY	NOMENCLATURE	FEDERAL STOCK NUMBER	TOOL NUMBER
1	H	AUDIO OSCILLATOR, HEWLETT PACKARD 200CD		
2	H	MULTIMETR, SIMPSON 269		
3	H	OSCILLOSCOPE, HEWLETT PACKARD 140A		
4	H	DUAL TRACE UNIT, HEWLETT PACKARD 1405A		
5	H	TIME BASE UNIT, HEWLETT PACKARD 1421A		
6	H	VOLTAGE DIVIDER PROBE, HEWLETT PACKARD C0-2-10003A/B		
7	H	ELECTRONIC FREQUENCY COUNTER, HEWLETT PACKARD 5245L		
8	H	ELECTRONIC FREQUENCY COUNTER HEWLETT PACKARD 5253B		
9	F, H	TOOL KIT, TECHNICIANS, RADIO		
10	H	MODULE REMOVER, RADIATION 106338-1		

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D. C., 29 September 1969

TM 11-6625-1565-15 is published for the use of all concerned.

By Order of the Secretary of the Army:

W. C. WESTMORELAND,
General, United States Army,
Chief of Staff

Official:

Active Army:

USAMB (5)
USACDCEC (5)
Eighth USA (5)
1st LOGCOMD (5)
2nd LOGCOMD (5)
9th LOGCOMD (5)
USACDCCEA (1)
USACDCCEA
Ft Huachuca (1)
SAAD (5)
TOAD (5)
LEAD (5)

NG: None.

USAR: None.

For explanation of abbreviation used, see AR 320-50.

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

SOMETHING WRONG WITH PUBLICATION

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE

BE EXACT PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE, TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT.

PRINTED NAME, GRADE OR TITLE AND TELEPHONE NUMBER	SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE.

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

The Metric System and Equivalents

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3,280.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 decagram = 10 grams = .35 ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Liquid Measure

1 centiliter = 10 milliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3.38 fl. ounces
1 liter = 10 deciliters = 33.81 fl. ounces
1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons

Square Measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. inch
1 sq. decimeter = 100 sq. centimeters = 15.5 sq. inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 sq. feet
1 sq. dekameter (are) = 100 sq. meters = 1,076.4 sq. feet
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 sq. hectometers = .386 sq. mile

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu. inches
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Approximate Conversion Factors

To change	*To*	*Multiply by*	*To change*	*To*	*Multiply by*
inches	centimeters	2.540	ounce-inches	Newton-meters	.007062
feet	meters	.305	centimeters	inches	.394
yards	meters	.914	meters	feet	3.280
miles	kilometers	1.609	meters	yards	1.094
square inches	square centimeters	6.451	kilometers	miles	.621
square feet	square meters	.093	square centimeters	square inches	.155
square yards	square meters	.836	square meters	square feet	10.764
square miles	square kilometers	2.590	square meters	square yards	1.196
acres	square hectometers	.405	square kilometers	square miles	.386
cubic feet	cubic meters	.028	square hectometers	acres	2.471
cubic yards	cubic meters	.765	cubic meters	cubic feet	35.315
fluid ounces	milliliters	29,573	cubic meters	cubic yards	1.308
pints	liters	.473	milliliters	fluid ounces	.034
quarts	liters	.946	liters	pints	2.113
gallons	liters	3.785	liters	quarts	1.057
ounces	grams	28.349	liters	gallons	.264
pounds	kilograms	.454	grams	ounces	.035
short tons	metric tons	.907	kilograms	pounds	2.205
pound-feet	Newton-meters	1.356	metric tons	short tons	1.102
pound-inches	Newton-meters	.11296			

Temperature (Exact)

°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

PIN: 019330-000